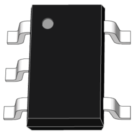
TSU111, TSU112, TSU114

Datasheet

Nanopower (900 nA), high accuracy (150 µV) 5 V CMOS operational amplifier


DFN6 1.2x1.3

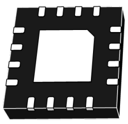

DFN8 2x2


SC70-5

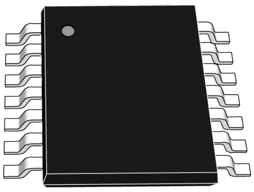
TSU111


MiniSO8

TSU112


QFN16 3x3

TSU114


TSSOP14

TSU114

Product status link
TSU111, TSU112, TSU114

Related products	
See TSU101, TSU102, and TSU104	for further power savings
See TSZ121, TSZ122, TSZ124	for increased accuracy

Features

- Sub-micro ampere current consumption: Icc = 900 nA typ. at 25 °C
- Low offset voltage: 150 µV max. at 25 °C, 235 µV max. over full temperature range (-40 to 85 °C)
- Low noise over 0.1 to 10 Hz bandwidth: 3.6 µVpp
- Low supply voltage: 1.5 V to 5.5 V
- Rail-to-rail input and output
- Gain bandwidth product: 11.5 kHz typ.
- Low input bias current: 10 pA max. at 25 °C
- High tolerance to ESD: 4 kV HBM
- More than 25 years of typical equivalent lifetime supplied by a 220 mA.h CR2032 coin type Lithium battery
- High accuracy without calibration
- Tolerance to power supply transient drops

Applications

- Gas sensors: CO, O_2, and H_2S
- Alarms: PIR sensors
- Signal conditioning for energy harvesting and wearable products
- Ultra long-life battery-powered applications
- Battery current sensing
- Active RFID tags

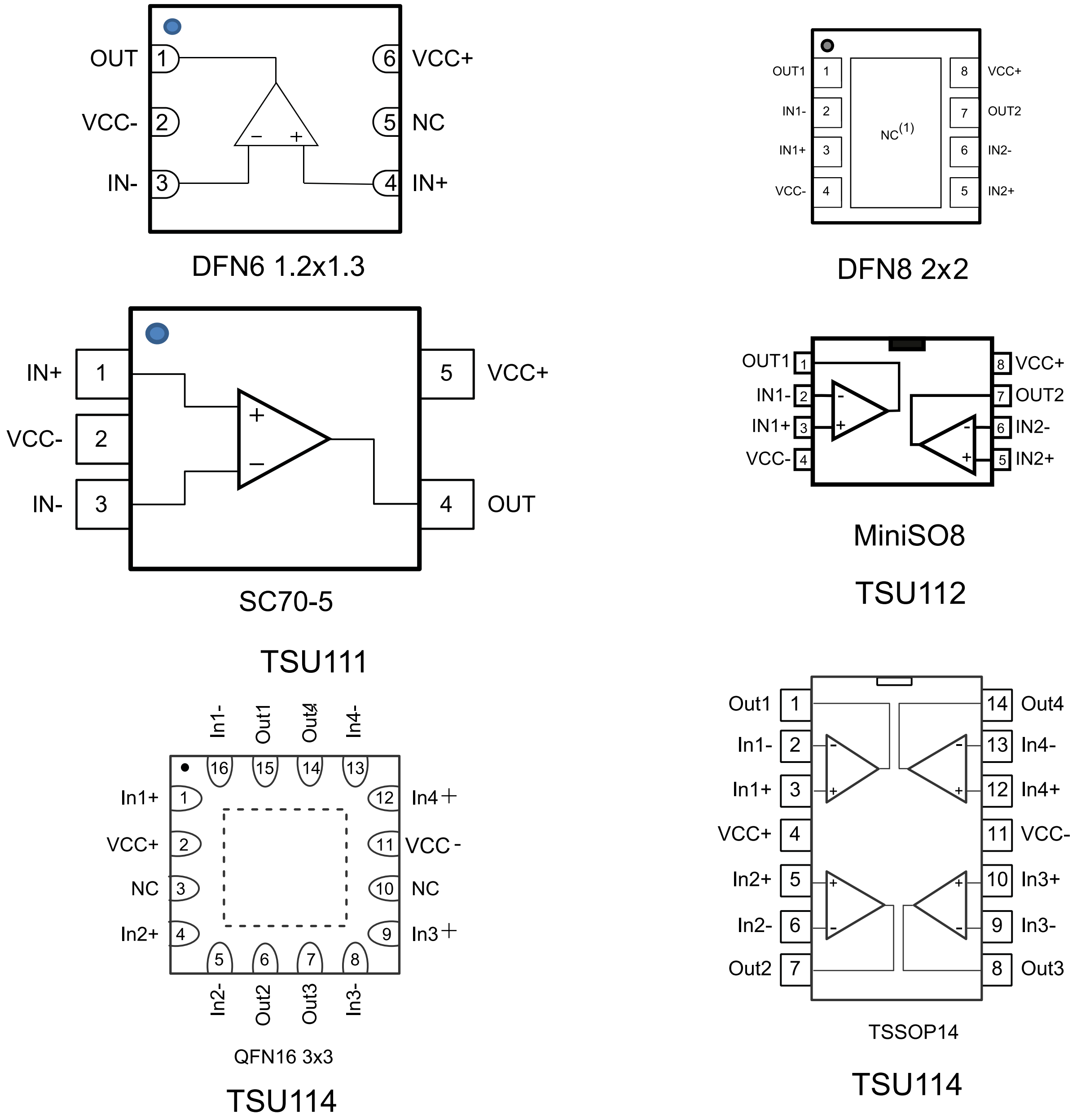
Description

The TSU111, TSU112 and the TSU114 operational amplifiers (op-amp) offer an ultra low-power consumption per channel of 900 nA typical and 1.2 µA maximum when supplied by 3.3 V. Combined with a supply voltage range of 1.5 V to 5.5 V, these features allow the TSU11x to be efficiently supplied by a coin type Lithium battery or a regulated voltage in low-power applications.

The high accuracy of 150 µV max. and 11.5 kHz gain bandwidth make the TSU11x ideal for sensor signal conditioning, battery supplied, and portable applications.

1 Package pin connections

Figure 2. Pin connections for each package (top view)



1. The exposed pad of the DFN8 2x2 can be connected to V_{CC-} or left floating.

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (2)		$\pm V_{CC}$	
V_{in}	Input voltage (3)		$(V_{CC -}) - 0.2$ to $(V_{CC +}) + 0.2$	
I_{in}	Input current (4)		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction-to-ambient (5) (6)	DFN6 1.2x1.3	232	°C/W
		SC70-5	205	
		DFN8 2x2	57	
		MiniSO8	190	
		QFN16 3x3	45	
		TSSOP14	100	
ESD	HBM: human body model (7)		4000	V
	CDM: charged device model (8)		1500	
	Latch-up immunity (9)		200	mA

1. *All voltage values, except the differential voltage are with respect to the network ground terminal.*
2. *The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.*
3. *$(V_{CC+}) - V_{in}$ must not exceed 6 V, $V_{in} - (V_{CC-})$ must not exceed 6 V.*
4. *The input current must be limited by a resistor in-series with the inputs.*
5. *R_{th} are typical values.*
6. *Short-circuits can cause excessive heating and destructive dissipation.*
7. *Related to ESDA/JEDEC JS-001 Apr. 2010.*
8. *Related to JEDEC JESD22-C101-E Dec. 2009.*
9. *Related to JEDEC JESD78C Sep. 2010.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common-mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$	
T_{oper}	Operating free-air temperature range	-40 to 85	°C

3 Electrical characteristics

Table 3. Electrical characteristics at (V_{CC+}) = 1.8 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			150	µV
		-40 °C < T< 85 °C			235	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 85 °C			1.4	µV/°C
I_{io}	Input offset current (1)	T = 25 °C		1	10	pA
		-40 °C < T< 85 °C			50	
I_{ib}	Input bias current (1)	T = 25 °C		1	10	
		-40 °C < T< 85 °C			50	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 1.8 V	T = 25 °C	76	107		dB
		-40 °C < T< 85 °C	71			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	95	120		
		R_L = 100 kΩ, -40 °C < T< 85 °C	90			
V_{OH}	High-level output voltage, (drop from V_{CC}+)	R_L = 10 kΩ, T = 25 °C		10	25	mV
		R_L = 10 kΩ, -40 °C < T< 85 °C			40	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25°C		8	25	
		R_L = 10 kΩ, -40 °C < T< 85 °C			40	
I_{out}	Output sink current, V_{out} = V_{CC} , V_{ID} = -200 mV	T = 25 °C	2.8	5		mA
		-40 °C < T< 85 °C	1.5			
	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	2	4		
		-40 °C < T< 85 °C	1.5			
I_{CC}	Supply current (per channel), no load, V_{out} = V_{CC}/2	T = 25 °C		900	1200	nA
		-40 °C < T< 85 °C			1480	
AC performance						
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		10		kHz
F_u	Unity gain frequency			8		
Φ_m	Phase margin			60		degrees
G_m	Gain margin			10		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V		2.5		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		220		nV/√Hz
$\int e_n$	Low-frequency, peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		3.8		μV_{pp}
t_{rec}	Overload recovery time	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T< 85 °C		325		µs

1. *Guaranteed by design*

Table 4. Electrical characteristics at (V_{CC+}) = 3.3 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			150	µV
		-40 °C < T< 85 °C			235	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 85 °C			1.4	µV/°C
I_{io}	Input offset current (1)	T = 25 °C		1	10	pA
		-40 °C < T< 85 °C			50	
I_{ib}	Input bias current (1)	T = 25 °C		1	10	
		-40 °C < T< 85 °C			50	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 3.3 V	T = 25 °C	81	110		dB
		-40 °C < T< 85 °C	76			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	105	130		
		R_L = 100 kΩ, -40 °C < T< 85 °C	105			
V_{OH}	High-level output voltage, (drop from V_{CC+})	R_L = 10 kΩ, T = 25 °C		10	25	mV
		R_L = 10 kΩ, -40 °C < T< 85 °C			40	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25°C		7	25	
		R_L = 10 kΩ, -40 °C < T< 85 °C			40	
I_{out}	Output sink current, V_{out} = V_{CC} , V_{ID} = -200 mV	T = 25 °C	12	22		mA
		-40 °C < T< 85 °C	6			
	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	9	18		
		-40 °C < T< 85 °C	5			
I_{CC}	Supply current (per channel), no load, V_{out} = V_{CC}/2	T = 25 °C		900	1200	nA
		-40 °C < T< 85 °C			1480	
AC performance						
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		11		kHz
F_u	Unity gain frequency			10		
Φ_m	Phase margin			60		degrees
G_m	Gain margin			7		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V		2.5		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		220		nV/√Hz
$\int e_n$	Low-frequency, peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		3.7		μV_{pp}
t_{rec}	Overload recovery time	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T< 85 °C		630		µs

1. *Guaranteed by design*

Table 5. Electrical characteristics at (V_{CC+}) = 5 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			150	µV
		-40 °C < T< 85 °C			235	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 85 °C			1.4	µV/°C
I_{io}	Input offset current [1]	T = 25 °C		1	10	pA
		-40 °C < T< 85 °C			50	
I_{ib}	Input bias current [1]	T = 25 °C		1	10	
		-40 °C < T< 85 °C			50	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 3.9 V	T = 25 °C	90	121		dB
		-40 °C < T< 85 °C	90			
	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 5 V	T = 25 °C	85	112		
		-40 °C < T< 85 °C	80			
SVR	Supply voltage rejection ratio, V_{CC} = 1.5 to 5.5 V, V_{icm} = 0 V	T = 25 °C	92	116		
		-40 °C < T< 85 °C	84			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	105	135		
		R_L = 100 kΩ, -40 °C < T< 85 °C	101			
V_{OH}	High-level output voltage, (drop from V_{CC+})	R_L = 10 kΩ, T = 25 °C		10	25	mV
		R_L = 10 kΩ, -40 °C < T< 85 °C			40	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25°C		7	25	
		R_L = 10 kΩ, -40 °C < T< 85 °C			40	
I_{out}	Output sink current, V_{out} = V_{CC} , V_{ID} = -200 mV	T = 25 °C	30	45		mA
		-40 °C < T< 85 °C	15			
	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	25	41		
		-40 °C < T< 85 °C	18			
I_{CC}	Supply current (per channel), no load, V_{out} = $V_{CC}/2$	T = 25 °C		950	1350	nA
		-40 °C < T< 85 °C			1620	
AC performance						

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		11.5		kHz
F_u	Unity gain frequency			10		
Φ_m	Phase margin			60		degrees
G_m	Gain margin			7		dB
SR	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V		2.7		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		200		nV/√Hz
$\int e_n$	Low-frequency, peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		3.6		μV_{pp}
t_{rec}	Overload recovery time	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T< 85 °C		940		µs
EMIRR	Electromagnetic interference rejection ratio (2)	V_{in} = -10 dBm, f = 400 MHz		54		dB
		V_{in} = -10 dBm, f = 900 MHz		79		
		V_{in} = -10 dBm, f = 1.8 GHz		65		
		V_{in} = -10 dBm, f = 2.4 GHz		65		

1. *Guaranteed by design*
2. *Based on evaluations performed only in conductive mode on the TSU111ICT.*

4 Electrical characteristic curves

Figure 3. Supply current vs. supply voltage

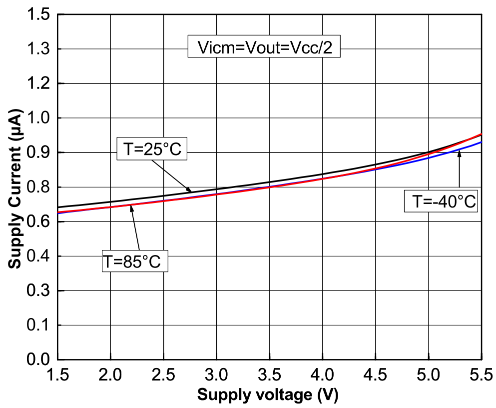


Figure 4. Supply current vs. input common-mode voltage

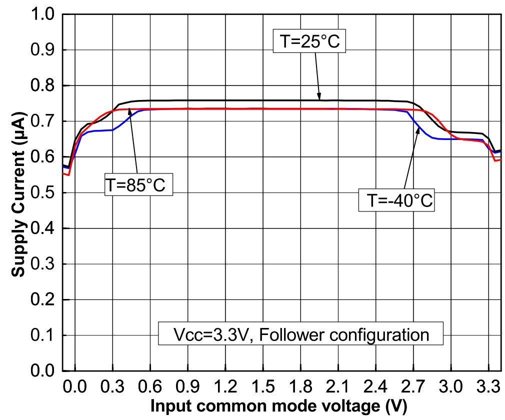


Figure 5. Input offset voltage vs. input common-mode voltage

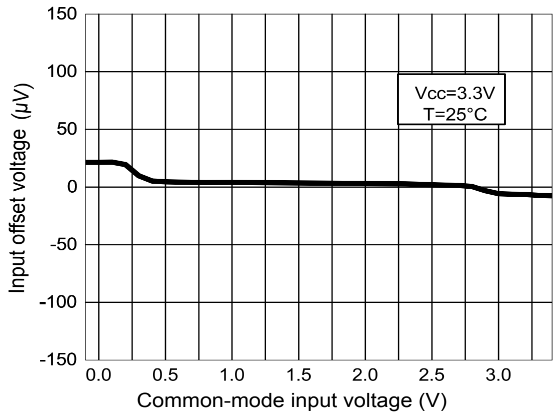


Figure 6. Input offset voltage distribution

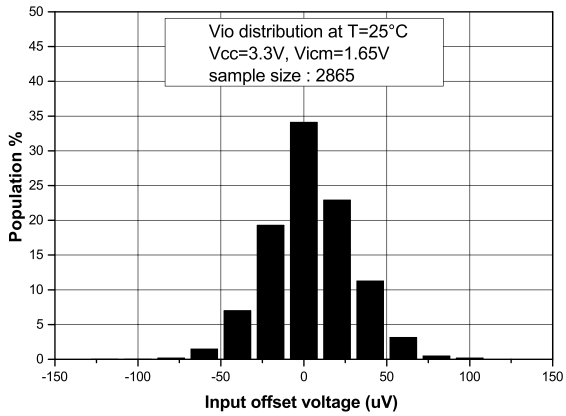


Figure 7. Input offset voltage vs. temperature at 3.3 V supply voltage

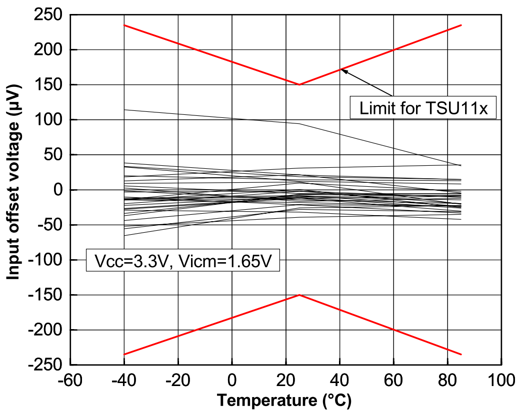


Figure 8. Input offset voltage temperature coefficient distribution from -40 °C to 25 °C

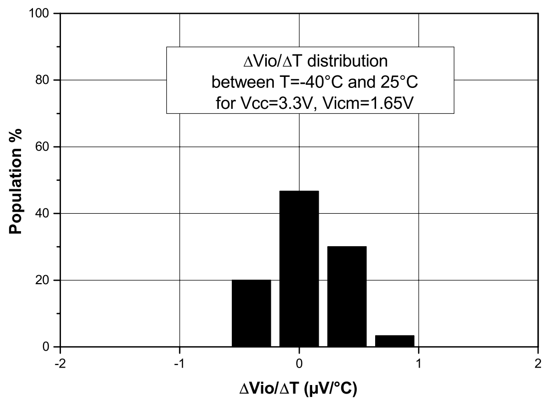


Figure 9. Input offset voltage temperature coefficient distribution from 25 °C to 85 °C

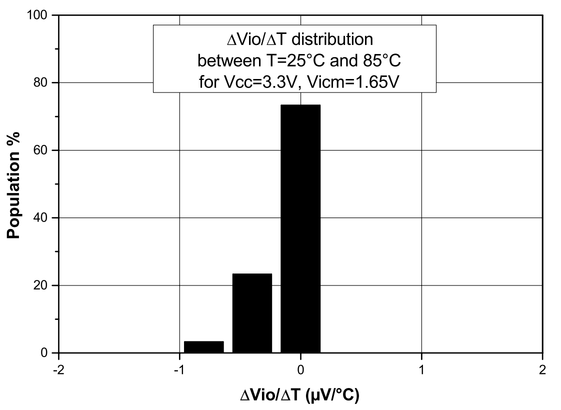


Figure 10. Input bias current vs. temperature at mid V_{ICM}

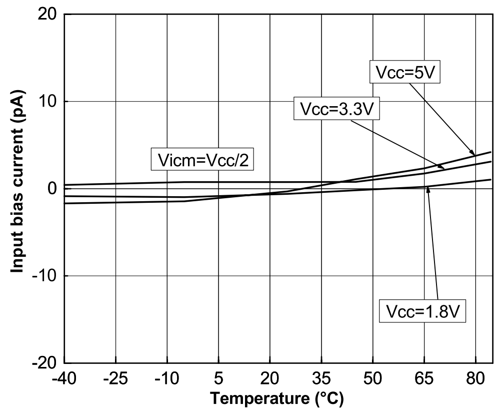


Figure 11. Input bias current vs. temperature at low V_{ICM}

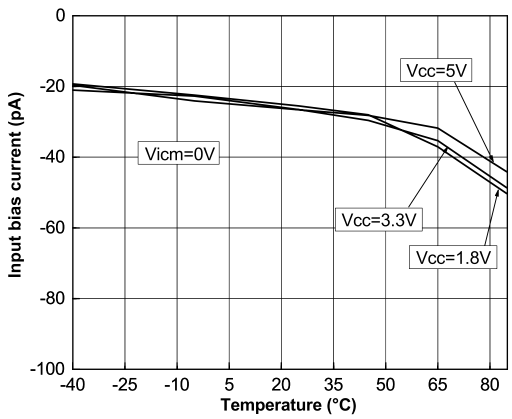


Figure 12. Input bias current vs. temperature at high V_{ICM}

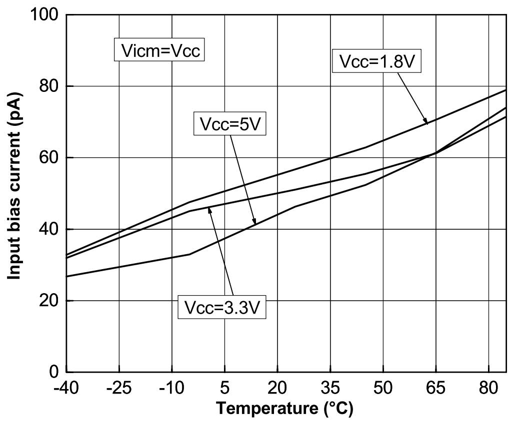


Figure 13. Output characteristics at 1.8 V supply voltage

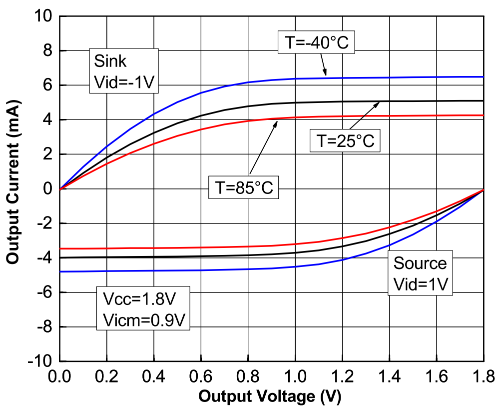


Figure 14. Output characteristics at 3.3 V supply voltage

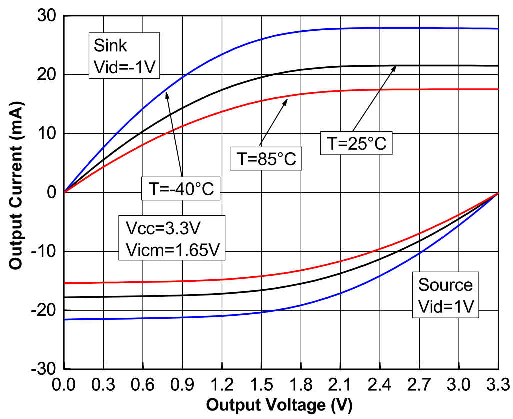


Figure 15. Output characteristics at 5 V supply voltage

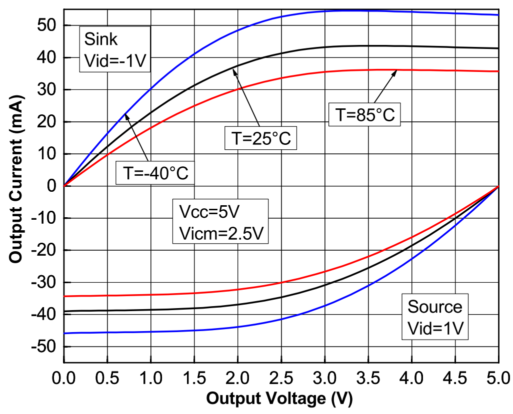


Figure 16. Output saturation with a sinewave on the input

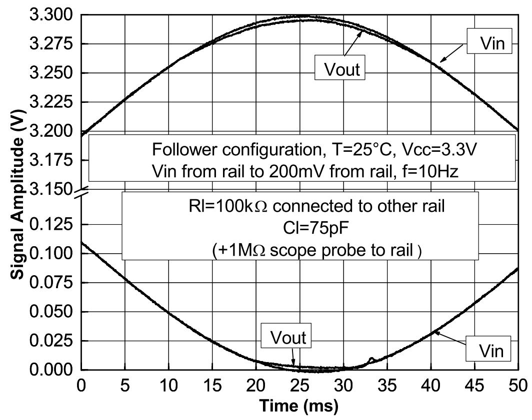


Figure 17. Output saturation with a square wave on the input

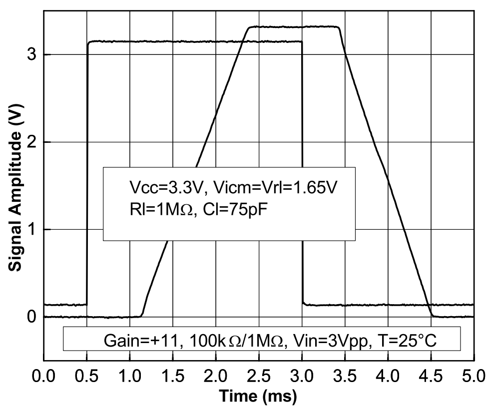


Figure 18. Phase reversal free

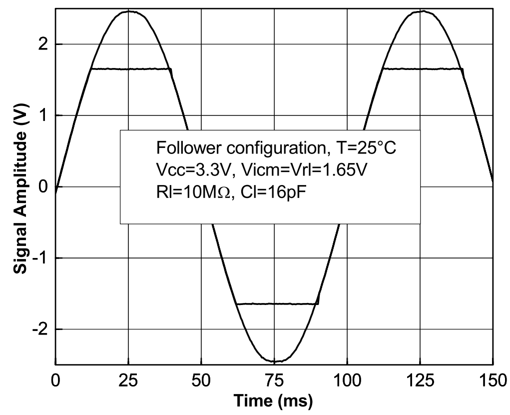


Figure 19. Slew rate vs. supply voltage

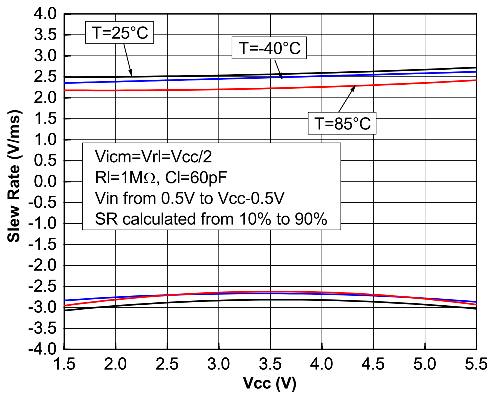


Figure 20. Output swing vs. input signal frequency

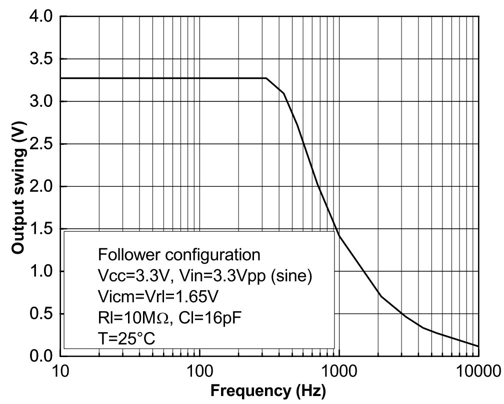


Figure 21. Triangulation of a sine wave

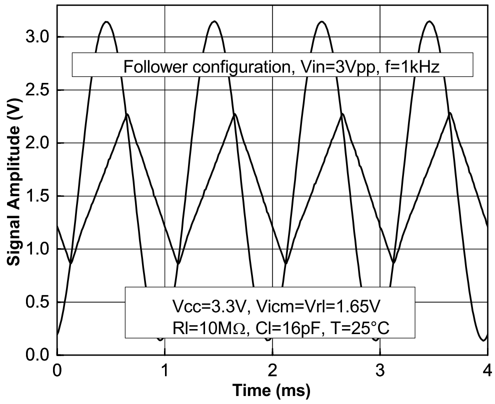


Figure 22. Large signal response at 3.3 V supply voltage

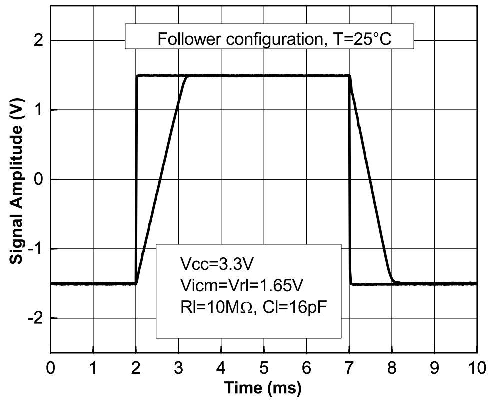


Figure 23. Small signal response at 3.3 V supply voltage

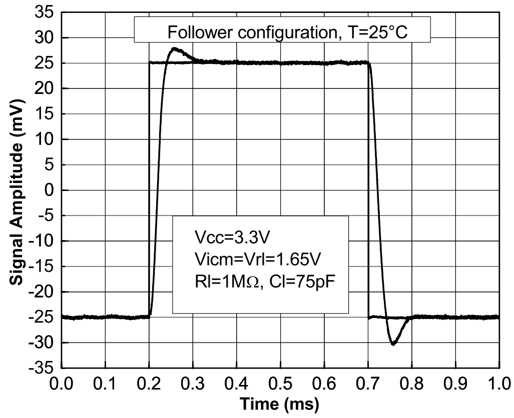


Figure 24. Overshoot vs. capacitive load at 3.3 V supply voltage

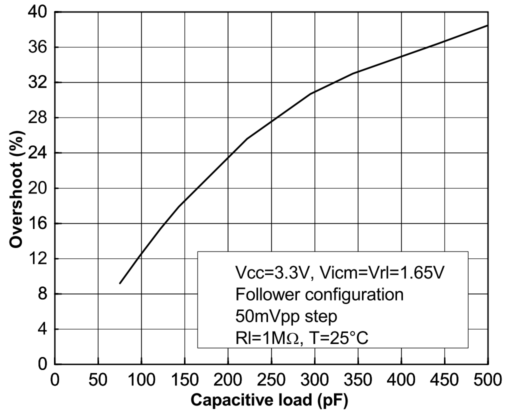


Figure 25. Open loop output impedance vs. frequency

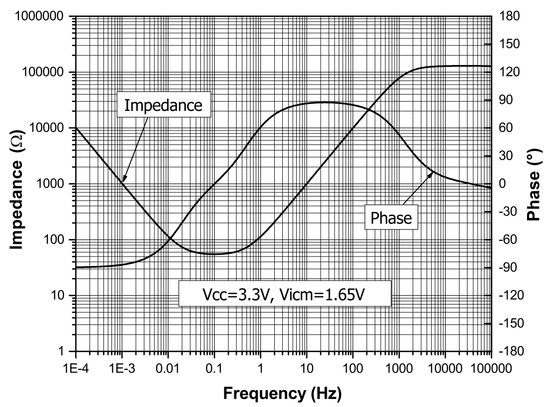


Figure 26. Bode diagram at 1.8 V supply voltage

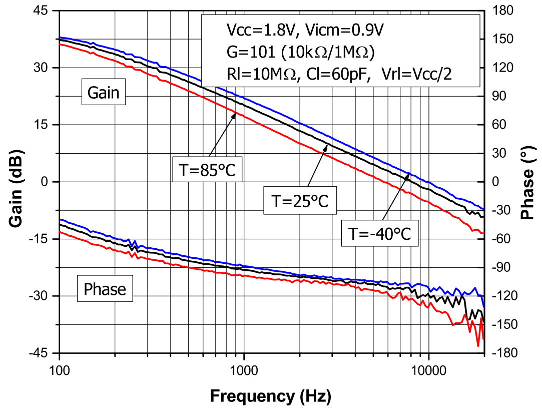


Figure 27. Bode diagram at 3.3 V supply voltage

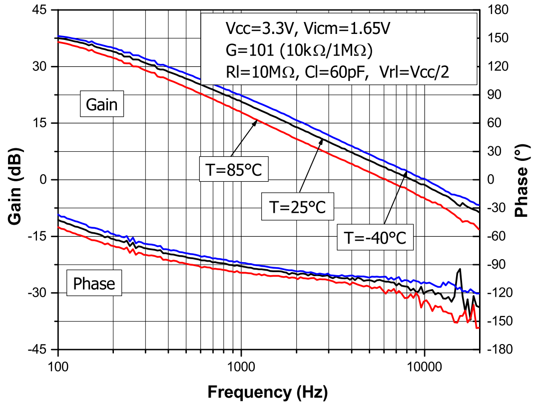


Figure 28. Bode diagram at 5 V supply voltage

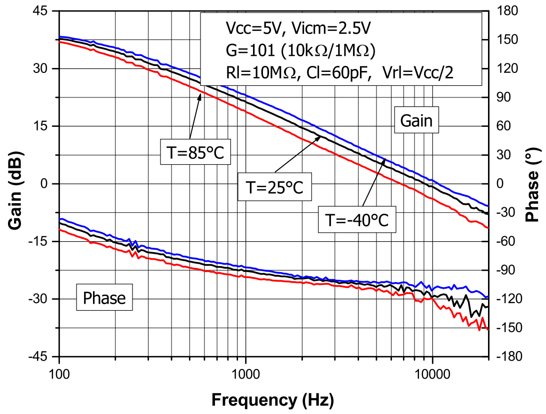


Figure 29. Gain bandwidth product vs. input common-mode voltage

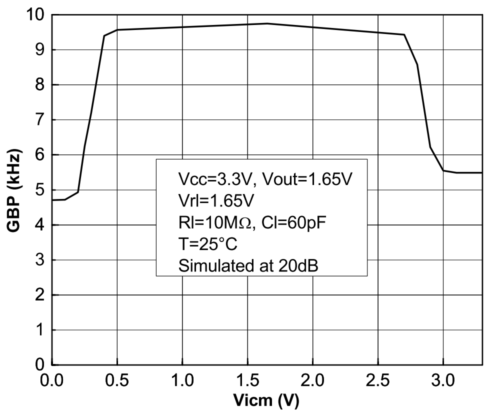


Figure 30. In-series resistor (Riso) vs. capacitive load

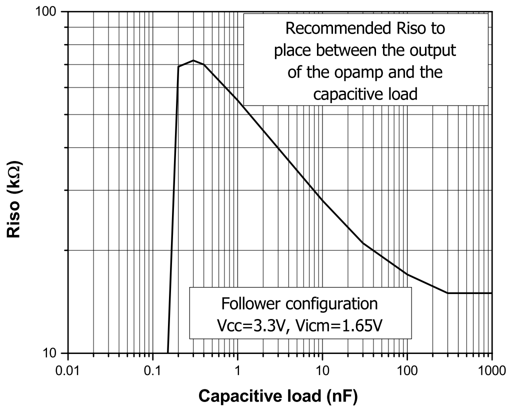


Figure 31. Noise vs. frequency for different power supply voltages

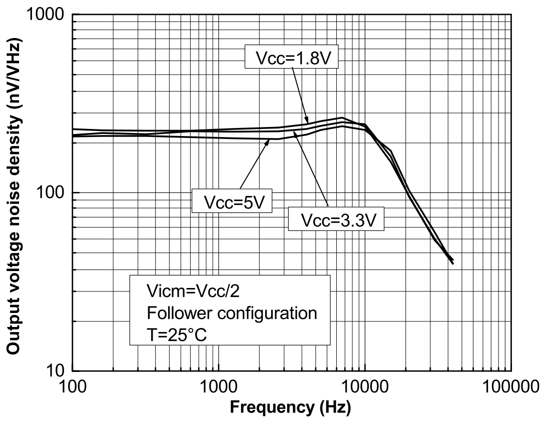


Figure 32. Noise vs. frequency for different common-mode input voltages

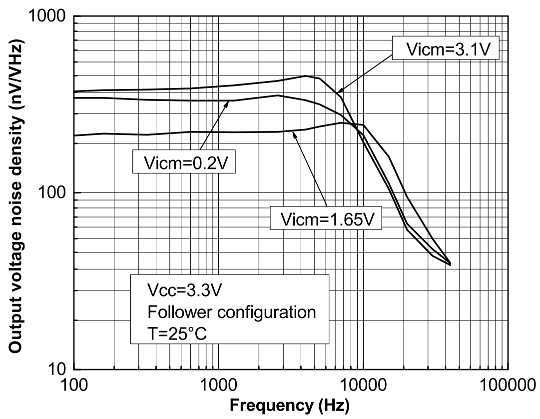
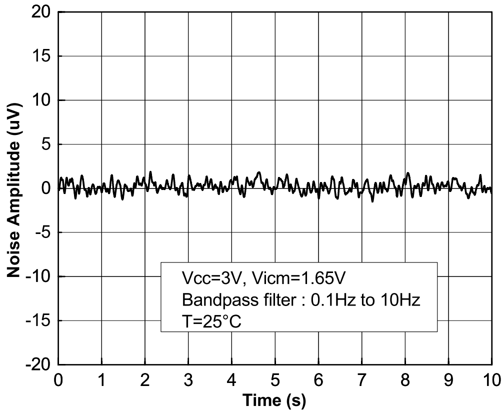


Figure 33. Noise amplitude on a 0.1 Hz to 10 Hz frequency range



5 Application information

5.1 Nanopower applications

The TSU11x can operate from 1.5 V to 5.5 V. The parameters are fully specified at 1.8 V, 3.3 V, and 5 V supply voltages and are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed on the industrial temperature range from -40 to 85 °C. The estimated lifetime of the TSU11x exceeds 25 years if supplied by a CR2032 battery (see Figure 34. CR2032 battery).

Figure 34. CR2032 battery

5.1.1 Schematic optimization aiming for nanopower

To benefit from the full performance of the TSU11x, the impedances must be maximized so that current consumption is not lost where it is not required.

For example, an aluminum electrolytic capacitance can have significantly high leakage. This leakage may be greater than the current consumption of the op-amp. For this reason, ceramic type capacitors are preferred.

For the same reason, big resistor values should be used in the feedback loop. However, there are two main limitations to be considered when choosing a resistor.

1. Noise generated: a 100 kΩ resistor generates 40 nV/√Hz, a bigger resistor value generates even more noise.
2. Leakage on the PCB: leakage can be generated by moisture. This can be improved by using a specific coating process on the PCB.

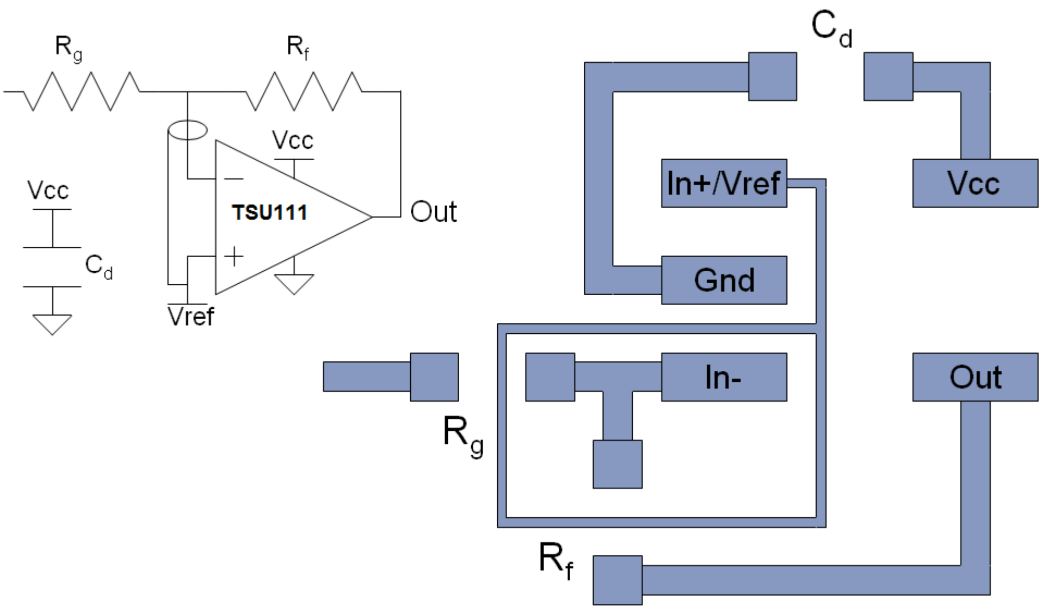
5.1.2 PCB layout considerations

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

Minimizing the leakage from sensitive high impedance nodes on the inputs of the TSU11x can be performed with a guarding technique. The technique consists of surrounding high impedance tracks by a low impedance track (the ring). The ring is at the same electrical potential as the high impedance node.

Therefore, even if some parasitic impedance exists between the tracks, no leakage current can flow through them as they are at the same potential (see Figure 35. Guarding on the PCB).

Figure 35. Guarding on the PCB



5.2 Rail-to-rail input

The TSU11x is built with two complementary PMOS and NMOS input differential pairs. Thus, the device has a rail-to-rail input, and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V.

The TSU11x has been designed to prevent phase reversal behavior.

5.3 Input offset voltage drift overtemperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using Equation 1.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

Where T = -40 °C and 85 °C.

The TSU11x datasheet maximum values are guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.4 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using Equation 2.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in Equation 3.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173 x 10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (°K)

T_S is the temperature of the die under temperature stress (°K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (Equation 4).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Equation 5 to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000\text{ h} \times 12\text{ months} / (24\text{ h} \times 365.25\text{ days})$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see Equation 6).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (Equation 7).

Equation 7

$$\Delta V_{io} = \frac{V_{io}\text{drift}}{\sqrt{(\text{months})}}$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

5.5 Using the TSU11x with sensors

The TSU11x has MOS inputs, thus input bias currents can be guaranteed down to 10 pA maximum at ambient temperature. This is an important parameter when the operational amplifier is used in combination with high impedance sensors.

The TSU11x is perfectly suited for trans-impedance configuration. This configuration allows a current to be converted into a voltage value with a gain set by the user. It is an ideal choice for portable electrochemical gas sensing or photo/UV sensing applications. The TSU11x, using trans-impedance configuration, is able to provide a voltage value based on the physical parameter sensed by the sensor.

5.5.1 Electrochemical gas sensors

The output current of electrochemical gas sensors is generally in the range of tens of nA to hundreds of µA. As the input bias current of the TSU11x is very low (see Figure 10. Figure 8, Figure 11. Figure 9, and Figure 12. Figure 10) compared to these current values, the TSU11x is well adapted for use with the electrochemical sensors of two or three electrodes. Figure 37. Potentiostat schematic using the TSU111 shows a potentiostat (electronic hardware required to control a three electrode cell) schematic using the TSU11x. In such a configuration, the devices minimize leakage in the reference electrode compared to the current being measured on the working electrode.

Another great advantage of TSU11x versus the competition is its low noise for low frequencies (3.6 µVpp over 0.1 to 10 Hz), and low input offset voltage of 150 µV max. These improved parameters for the same power consumption allow a better accuracy.

Figure 36. Trans-impedance amplifier schematic

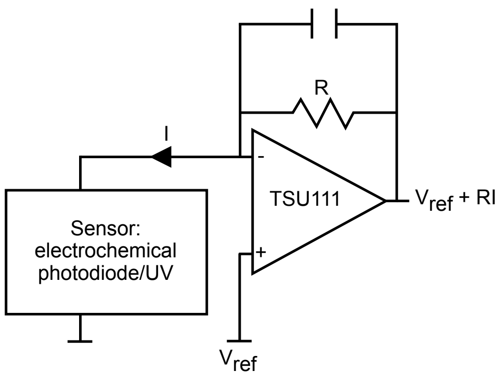
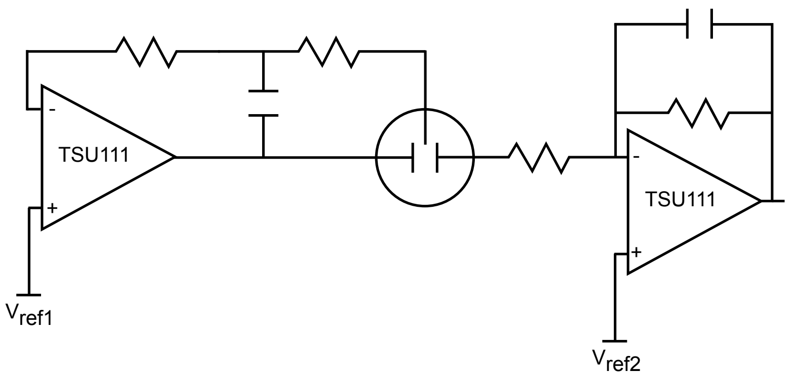


Figure 37. Potentiostat schematic using the TSU111



5.6 Fast desaturation

When the TSU11x goes into saturation mode, it takes a short period of time to recover, typically 630 µs. When recovering after saturation, the TSU11x does not exhibit any voltage peaks that could generate issues (such as false alarms) in the application (see Figure 16. Figure 14).

We can observe that this circuit still exhibits good gain even close to the rails i.e. A_{vd} greater than 105 dB for V_{cc} = 3.3 V with V_{out} varying from 200 mV up to a supply voltage minus 200 mV. With a trans-impedance schematic, a voltage reference can be used to keep the signal away from the supply rails.

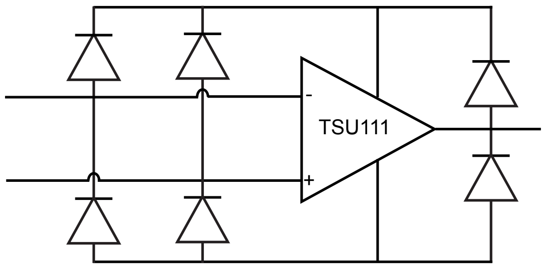
5.7 Using the TSU11x in comparator mode

The TSU11x can be used as a comparator. In this case, the output stage of the device always operates in saturation mode. In addition, Figure 4. Figure 3 shows that the current consumption is not higher and even decreases smoothly close to the rails. The TSU11x is obviously an operational amplifier and is therefore optimized for use in linear mode. We recommend using the TS88 series of nanopower comparators if the primary function is to perform a signal comparison only.

5.8 ESD structure of the TSU11x

The TSU11x is protected against electrostatic discharge (ESD) with dedicated diodes (see Figure 38. ESD structure). These diodes must be considered at application level especially when signals applied on the input pins go beyond the power supply rails (V_{CC+}) or (V_{CC-}).

Figure 38. ESD structure



Current through the diodes must be limited to a maximum of 10 mA as stated in Table 1. Absolute maximum ratings (AMR). A serial resistor on the inputs can be used to limit this current.

5.9 EMI robustness of nanopower devices

Nanopower devices exhibit higher impedance nodes and consequently they are more sensitive to EMI. To improve the natural robustness of the TSU11x device, we recommend to add three capacitors of around 22 pF each between the two inputs, and between each input and ground. These capacitors lower the impedance of the input at high frequencies and therefore reduce the impact of the radiation.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6.1 SC70-5 (or SOT323-5) package information (TSU111)

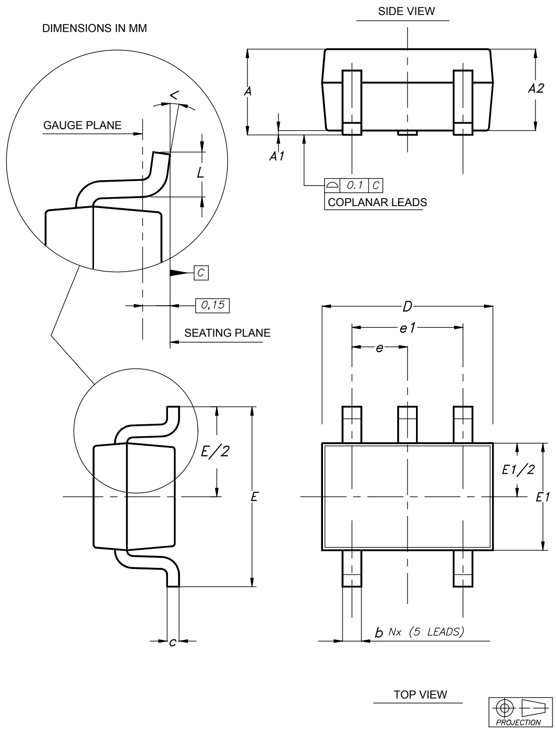


Figure 39. SC70-5 (or SOT323-5) package outline

Table 6. SC70-5 (or SOT323-5) package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

6.2 DFN6 1.2x1.3 package information (TSU111)

Figure 40. DFN6 1.2x1.3 package outline

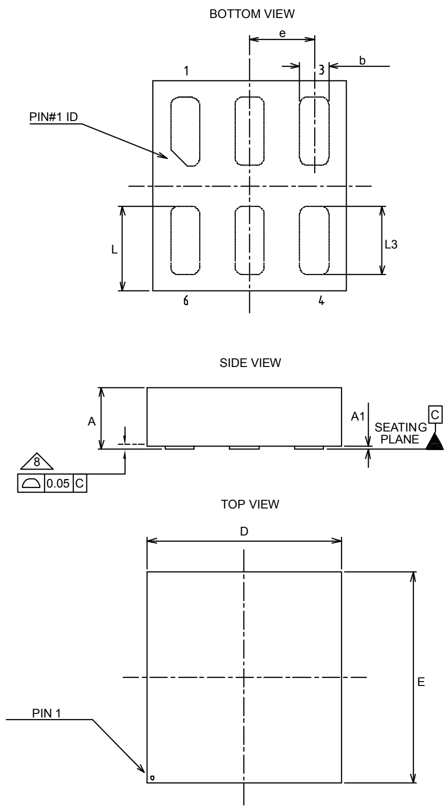


Table 7. DFN6 1.2x1.3 mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.31	0.38	0.40	0.012	0.015	0.016
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.18	0.25	0.006	0.007	0.010
c		0.05			0.002	
D		1.20			0.047	
E		1.30			0.051	
e		0.40			0.016	
L	0.475	0.525	0.575	0.019	0.021	0.023
L3	0.375	0.425	0.475	0.015	0.017	0.019

Figure 41. DFN6 1.2x1.3 recommended footprint

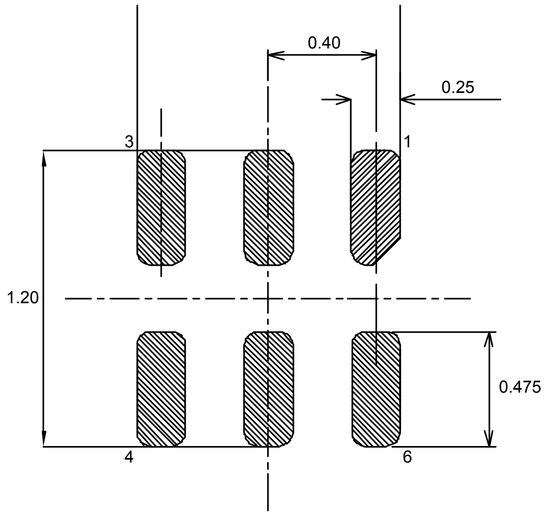


Table 8. DFN6 1.2x1.3 recommended footprint data

Dimensions		
Ref.	**Millimeters**	**Inches**
A	4.00	0.158
B		
C	0.50	0.020
D	0.30	0.012
E	1.00	0.039
F	0.70	0.028
G	0.66	0.026

6.3 MiniSO8 package information (TSU112)

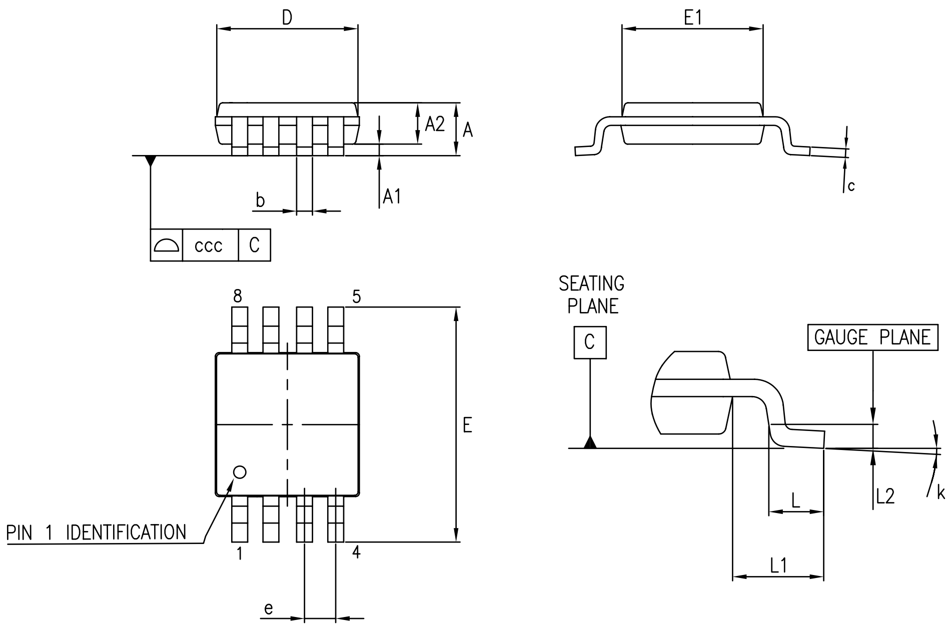


Figure 42. MiniSO8 package outline

Table 9. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

6.4 DFN8 2x2 package information (TSU112)

Figure 43. DFN8 2x2 package outline

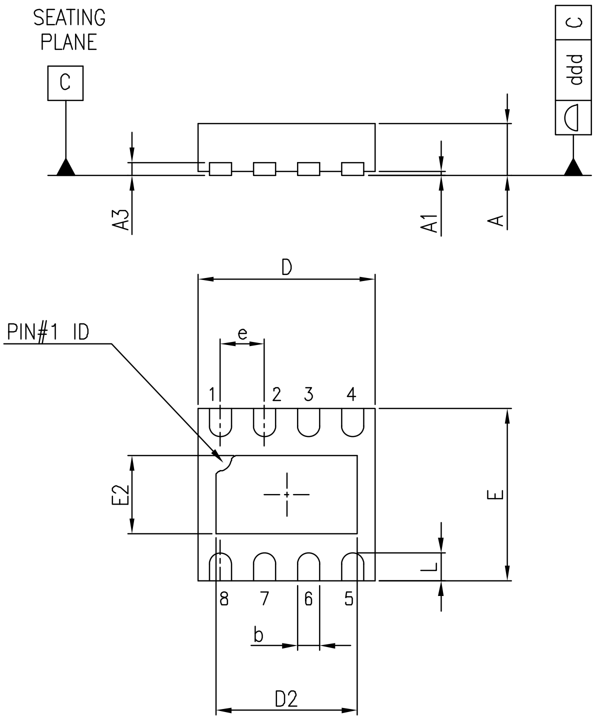


Table 10. DFN8 2x2 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

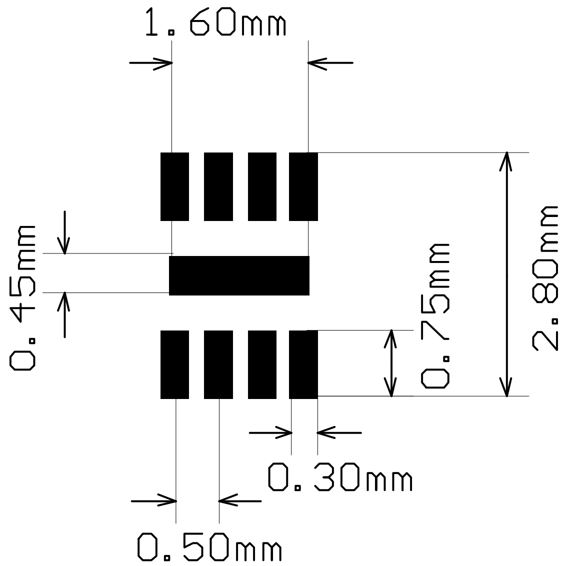


Figure 44. DFN8 2x2 recommended footprint

6.5 TSSOP14 package information (TSU114)

Figure 45. TSSOP14 package outline

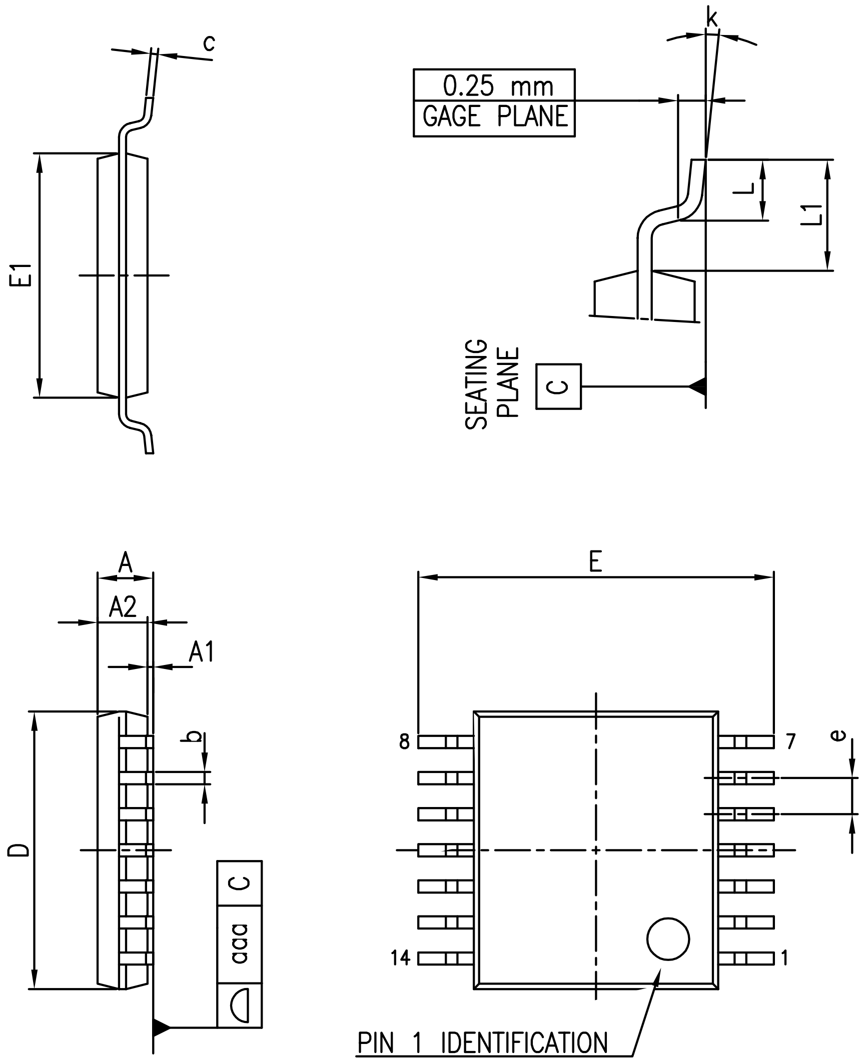


Table 11. TSSOP14 mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A			1.20
A1	0.05		0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0		8
aaa			0.10

6.6 QFN16 (3x3x0.9) package information (TSU114)

Figure 46. QFN16 (3x3x0.9) package outline

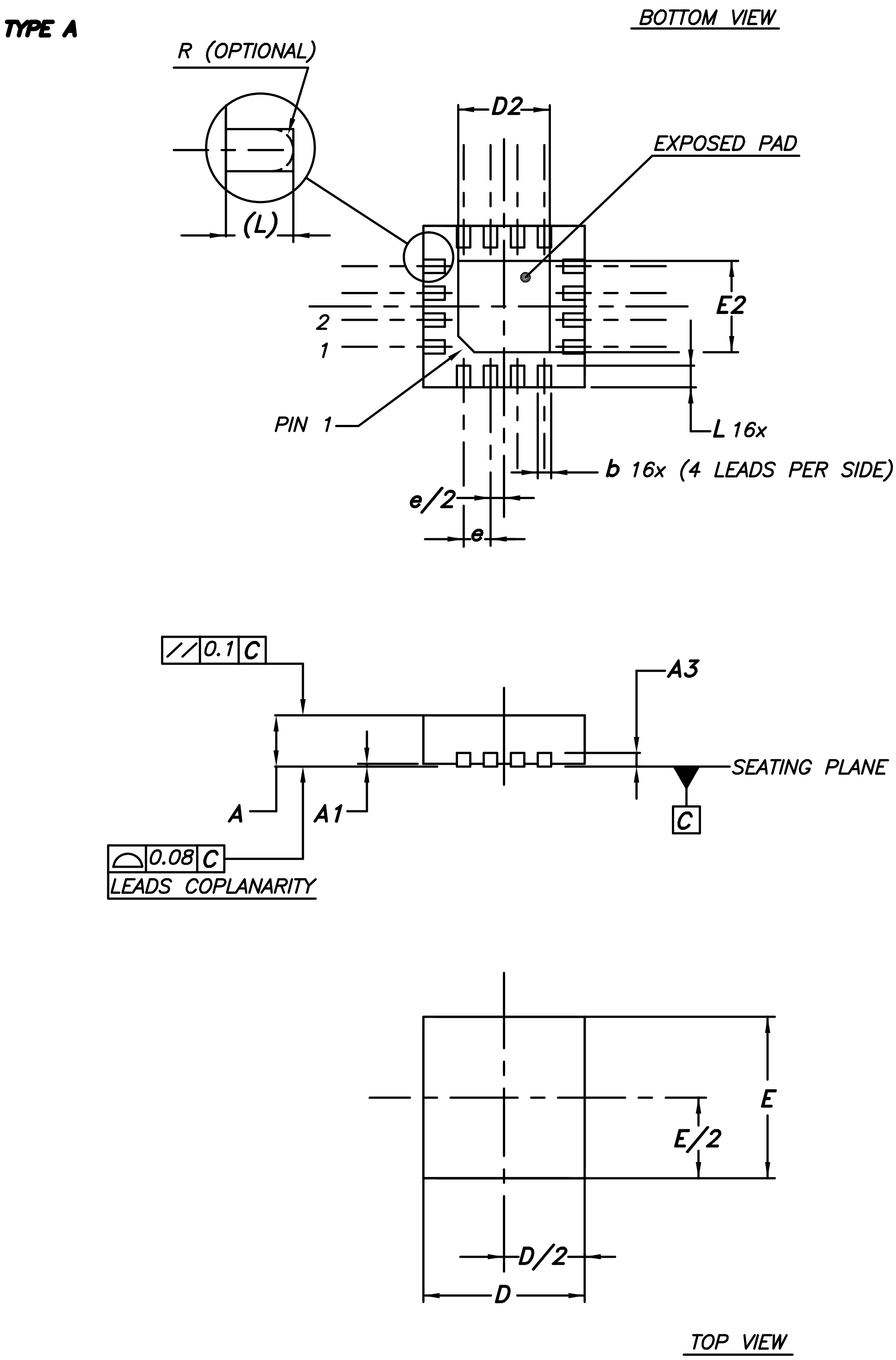


Table 12. **QFN16 (3x3x0.9) mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1
A1	0		0.05
A3		0.20	
b	0.18		0.30
D	2.90	3.00	3.10
D2	1.50		1.80
E	2.90	3.00	3.10
E2	1.50		1.80
e		0.50	
L(1)	0.30		0.50

1. *The value of "L" a JEDEC norm is min. 0.35 – max. 0.45*

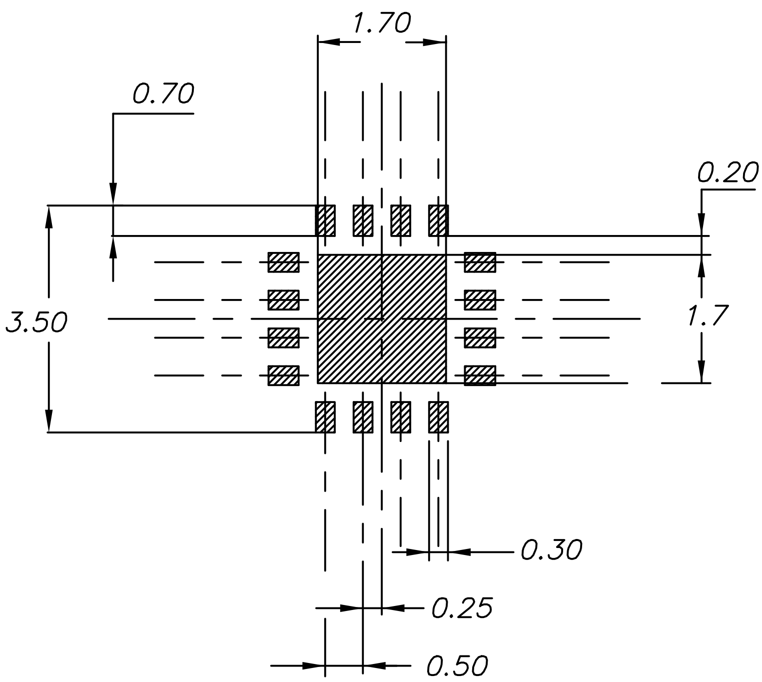


Figure 47. **QFN16 (3x3x0.9) recommended footprint**

7 Ordering information

Table 13. **Order code**

Order code	Temperature range	Package [1]	Marking
TSU111IQ1T	-40 °C to 85 °C	DFN6 1.2x1.3	K8
TSU111ICT		SC70-5	
TSU112IQ2T		DFN8 2x2	K37
TSU112IST		MiniSO8	
TSU114IPT		TSSOP14	TSU114IPT
TSU114IQ4T		QFN16 3x3x0.9	K164

1. *All devices are delivered in tape and reel packing.*

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
17-Oct-2016	1	Initial release
14-Nov-2016	2	Features: added "rail-to-rail input and output". Description: updated the maximum ultra low-power consumption of TSU111 op-amp. Applications: updated Table 5: added EMIRR typ. values Added Section 5.9: "EMI robustness of nanopower devices".
04-Dec-2017	3	Added the part number TSU112 and the relative package information MiniSO8 and DFN8 2x2.
08-May-2018	4	Updated Section 3 Electrical characteristics.
21-Jan-2019	5	Added the part number TSU114, therefore the document has been updated accordingly.
06-Feb-2019	6	Updated Section 3 Electrical characteristics. Added Figure 5. Input offset voltage vs. input common-mode voltage.

Contents

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