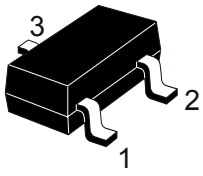
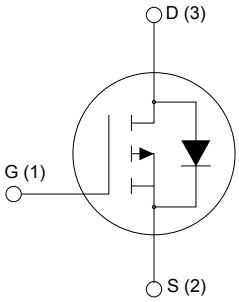
STR2P3LLH6

Datasheet

P-channel -30 V, 48 mΩ typ., -2 A STripFET™ H6 Power MOSFET in a SOT-23 package



SOT-23



PG1D3S2

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STR2P3LLH6	-30 V	56 mΩ	-2 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status
STR2P3LLH6

Product summary	
Order code	STR2P3LLH6
Marking	2K3L
Package	SOT-23
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_{pcb} = 25 °C	-2	A
I_D	Drain current (continuous) at T_{pcb} = 100 °C	-1.2	A
I_{DM} (1)	Drain current (pulsed)	-8	A
P_{TOT}	Total dissipation at T_{pcb} = 25 °C	0.35	W
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

1. *Pulse width limited by safe operating area*

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb, single operation	357	°C/W

1. *When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 s*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 3. On /off states

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = -30 V (1)			-1	µA
I_{GSS}	Gate body leakage current	V_{GS} = 0 V, V_{GS} = ±20 V			-100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = -10 V, I_D = -1 A V_{GS} = -4.5 V, I_D = -1 A		48 75	56 90	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{iss}	Input capacitance	V_{DS} = -25 V, f=1 MHz V_{GS} = 0 V	-	639	-	pF
C_{oss}	Output capacitance		-	79	-	
C_{rss}	Reverse transfer capacitance		-	52	-	
Q_g	Total gate charge	V_{DD} = -15 V, I_D = -2 A V_{GS} = -4.5 to 0 V (see Figure 13. Gate charge test circuit)	-	6	-	nC
Q_{gs}	Gate-source charge		-	1.9	-	
Q_{gd}	Gate-drain charge		-	2.1	-	

Table 5. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = -15 V, I_D = -2 A, R_G = 4.7 Ω, V_{GS} = -10 V (see Figure 12. Switching times test circuit for resistive load)	-	5.4	-	ns
t_r	Rise time		-	5	-	
$t_{d\ (off)}$	Turn-off delay time		-	19.2	-	
t_f	Fall time		-	3.4	-	

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = -2 A, V_{GS} = 0 V	-	-	-1.1	V

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{rr}	Reverse recovery time	I_{SD} = -2 A, di/dt = 100 A/µs, V_{DD}= 24 V, T_J = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	-	11.2	ns
Q_{rr}	Reverse recovery charge		-	-	3.5	nC
I_{RRM}	Reverse recovery current		-	-	-0.6	A

1. *Pulsed: pulse duration=300µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

Figure 1. Safe operating area

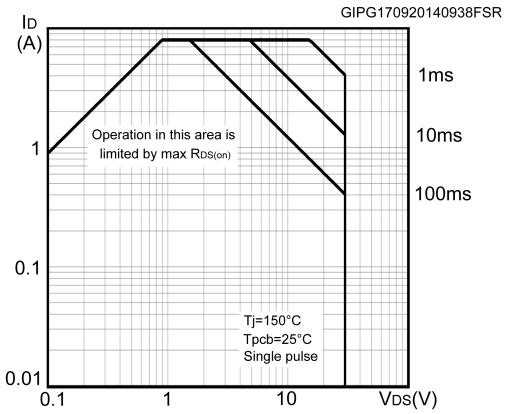


Figure 2. Thermal impedance

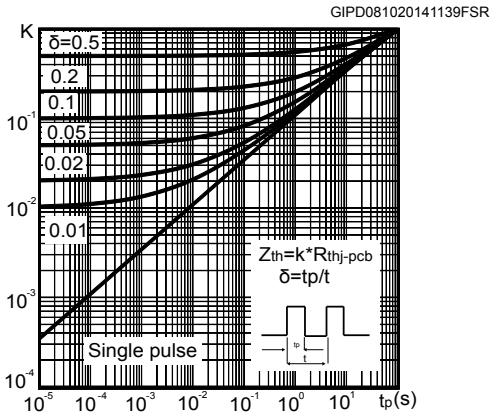


Figure 3. Output characteristics

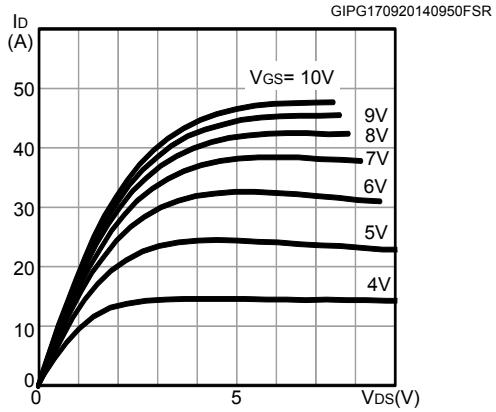


Figure 4. Transfer characteristics

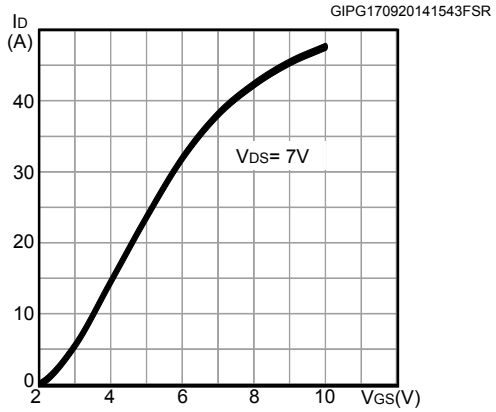


Figure 5. Gate charge vs gate-source voltage

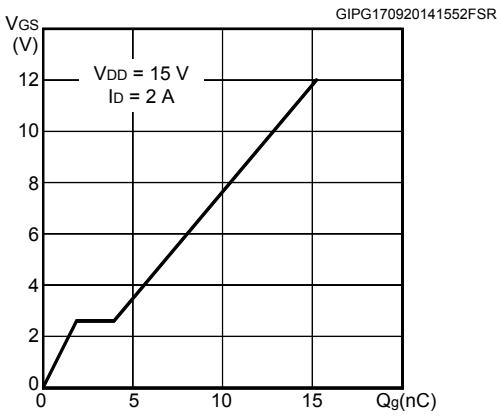


Figure 6. Static drain-source on-resistance

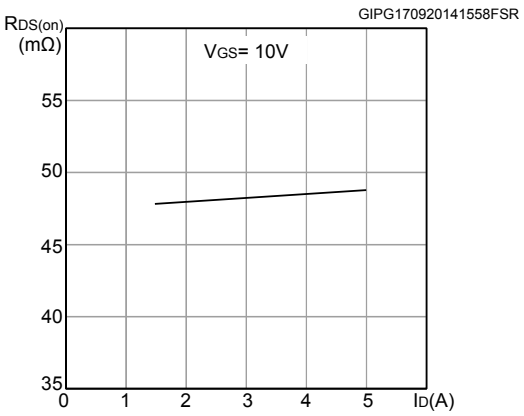


Figure 7. Normalized $V_{(BR)DSS}$ vs temperature

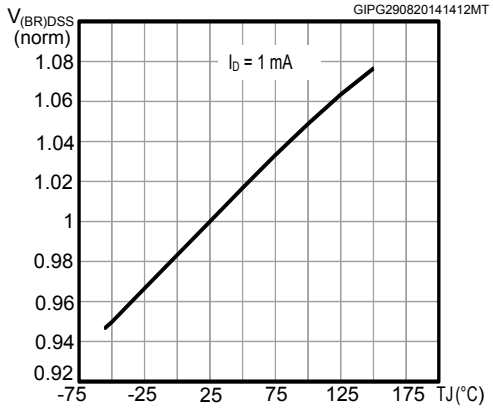


Figure 8. Capacitance variations

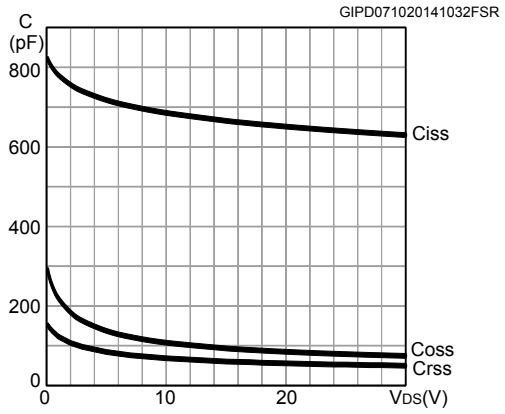


Figure 9. Normalized gate threshold voltage vs. temperature

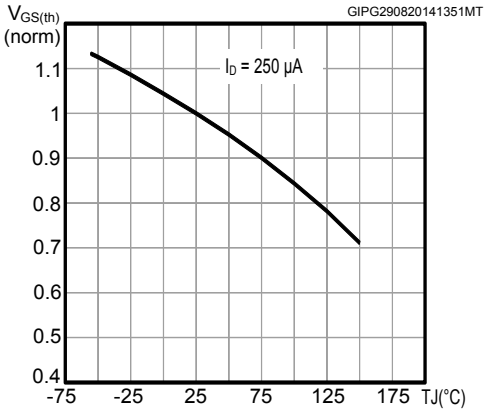


Figure 10. Normalized on-resistance vs. temperature

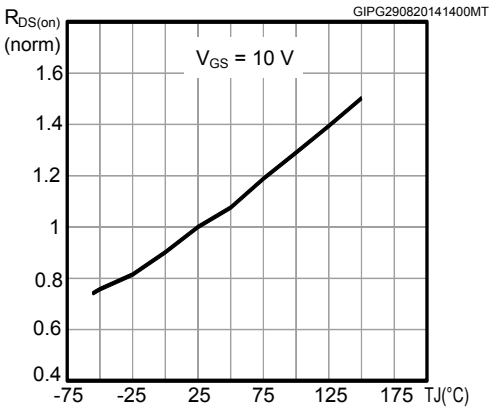
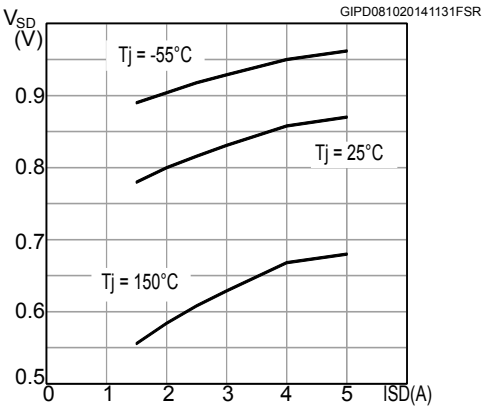


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Switching times test circuit for resistive load

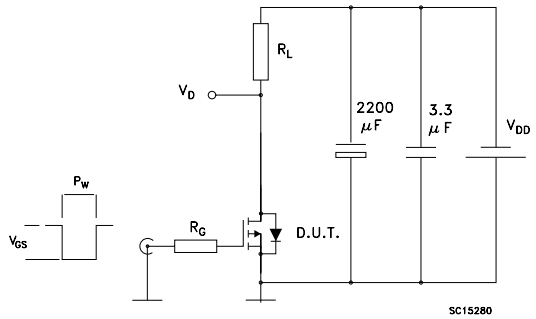


Figure 13. Gate charge test circuit

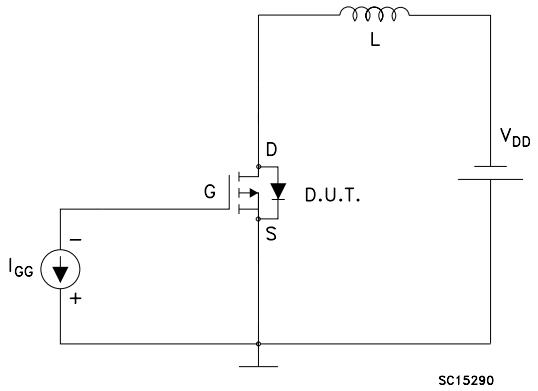
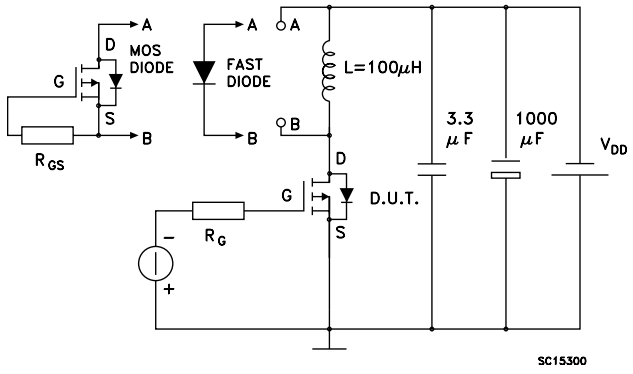


Figure 14. Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SOT-23 package information

Figure 15. SOT-23 package outline

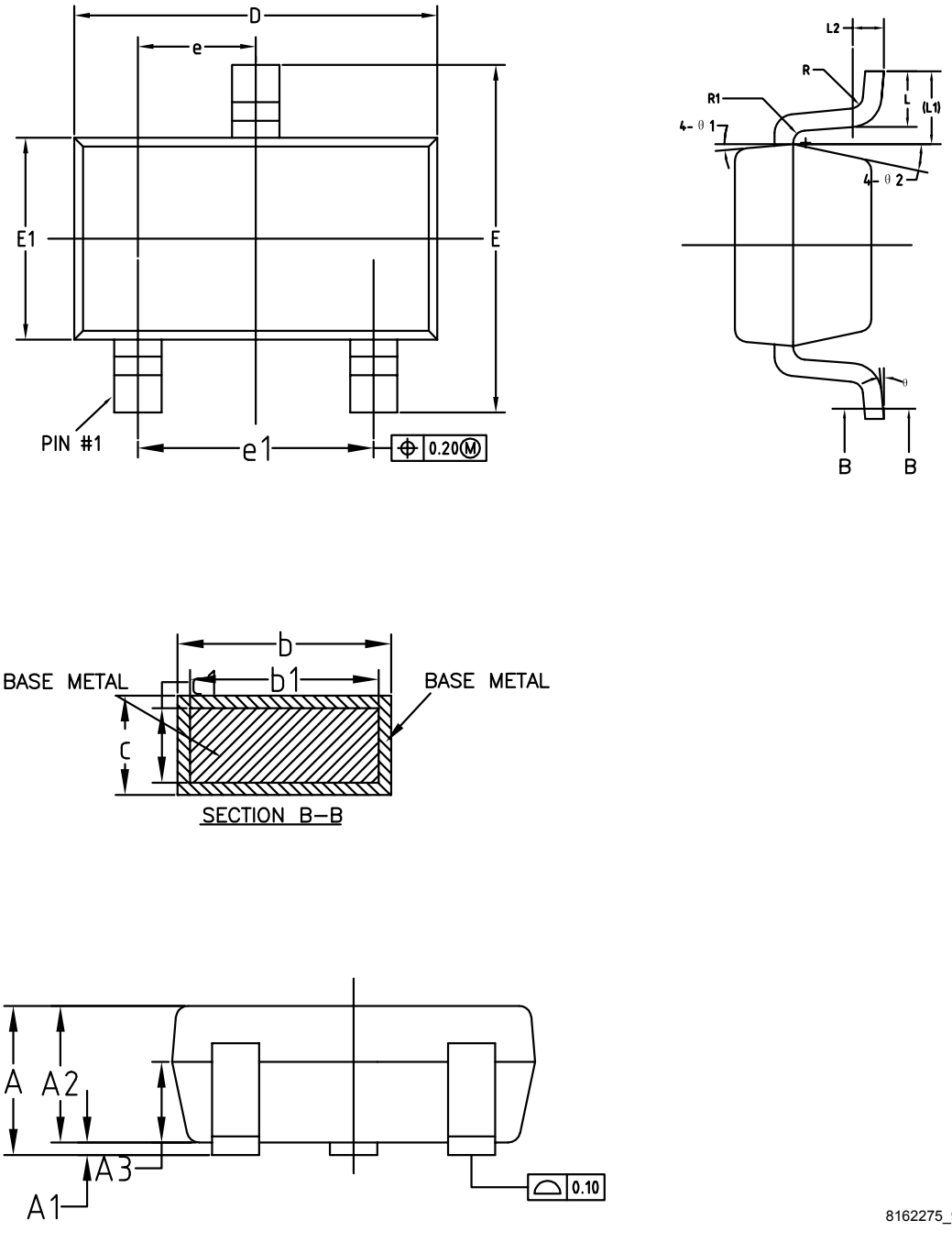
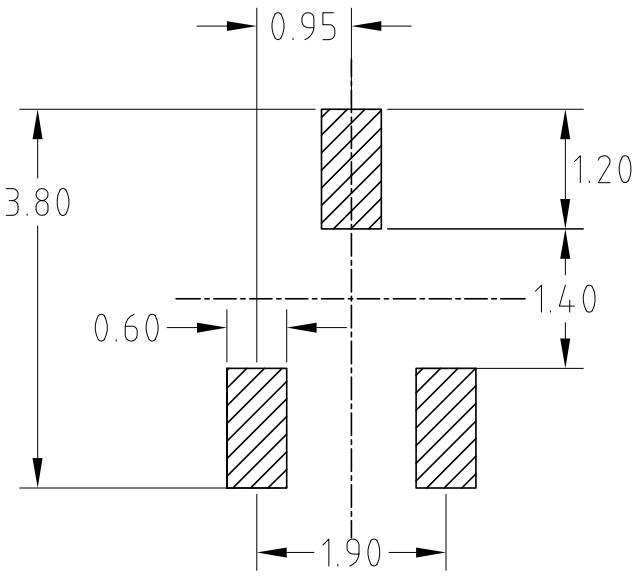


Table 7. **SOT-23 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.25
A1	0.00		0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36		0.50
b1	0.36	0.38	0.45
c	0.14		0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59 REF		
L2	0.25 BSC		
R	0.05		
R1	0.05		
θ	0°		8°
θ1	3°	5°	7°
θ2	6°		14°

Figure 16. **SOT-23 recommended footprint (dimensions are in mm)**



Revision history

Table 8. **Document revision history**

Date	Revision	Changes
09-May-2013	1	Initial release.
03-Nov-2014	2	Document status promoted from preliminary to production data. Added Section 2.1: "Electrical characteristics (curves)". Minor text changes.
05-Nov-2015	3	Updated title and features in cover page. Updated *Table 2: "Absolute maximum ratings"*, *Table 4: "On /off states"*, *Table 5: "Dynamic"*, *Table 6: "Switching times"*, *Table 7: "Source drain diode"* and *Section 2.1: "Electrical characteristics (curves)"*. Minor text changes.
21-Feb-2018	4	Removed maturity status indication from cover page. The document status is production data. Updated *Section 4.1 SOT-23 package information*. Minor text changes.
26-Mar-2019	5	Updated Table 3. On /off states. Minor text changes.

Contents