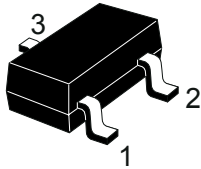
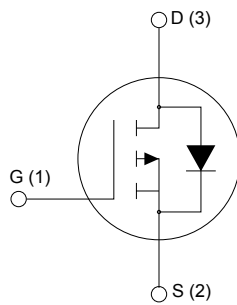


## P-channel -30 V, 48 mΩ typ., -2 A STripFET™ H6 Power MOSFET in a SOT-23 package



SOT-23



PG1D3S2


**Product status**

STR2P3LLH6

**Product summary**

|                   |               |
|-------------------|---------------|
| <b>Order code</b> | STR2P3LLH6    |
| <b>Marking</b>    | 2K3L          |
| <b>Package</b>    | SOT-23        |
| <b>Packing</b>    | Tape and reel |

### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STR2P3LLH6 | -30 V           | 56 mΩ                    | -2 A           |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter   | Value      | Unit             |
|----------------|---|------------|------------------|
| $V_{DS}$       | Drain-source voltage  | -30        | V                |
| $V_{GS}$       | Gate-source voltage   | $\pm 20$   | V                |
| $I_D$          | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$  | -2         | A                |
| $I_D$          | Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$ | -1.2       | A                |
| $I_{DM}^{(1)}$ | Drain current (pulsed)  | -8         | A                |
| $P_{TOT}$      | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$           | 0.35       | W                |
| $T_J$          | Operating junction temperature range                                | -55 to 150 | $^\circ\text{C}$ |
| $T_{stg}$      | Storage temperature range   |            | $^\circ\text{C}$ |

1. Pulse width limited by safe operating area

**Table 2. Thermal resistance**

| Symbol              | Parameter   | Value | Unit               |
|---------------------|---|-------|--------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb, single operation | 357   | $^\circ\text{C/W}$ |

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified).

**Table 3. On /off states**

| Symbol        | Parameter                         | Test conditions   | Min | Typ      | Max      | Unit             |
|---------------|-----------------------------------|---|-----|----------|----------|------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$   | -30 |          |          | V                |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = -30\text{ V}$ <sup>(1)</sup>                                  |     |          | -1       | $\mu\text{A}$    |
| $I_{GSS}$     | Gate body leakage current         | $V_{GS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$  |     |          | -100     | nA               |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$   | -1  |          | -2.5     | V                |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = -10\text{ V}$ , $I_D = -1\text{ A}$<br>$V_{GS} = -4.5\text{ V}$ , $I_D = -1\text{ A}$ |     | 48<br>75 | 56<br>90 | $\text{m}\Omega$ |

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

| Symbol    | Parameter                    | Test conditions   | Min | Typ | Max | Unit          |
|-----------|------------------------------|---|-----|-----|-----|---------------|
| $C_{ISS}$ | Input capacitance            | $V_{DS} = -25\text{ V}$ , $f = 1\text{ MHz}$<br>$V_{GS} = 0\text{ V}$ | -   | 639 | -   | $\mu\text{F}$ |
| $C_{OSS}$ | Output capacitance           |   | -   | 79  | -   |               |
| $C_{RSS}$ | Reverse transfer capacitance |   | -   | 52  | -   |               |
| $Q_g$     | Total gate charge            | $V_{DD} = -15\text{ V}$ , $I_D = -2\text{ A}$                         | -   | 6   | -   | nC            |
| $Q_{gs}$  | Gate-source charge           | $V_{GS} = -4.5\text{ to }0\text{ V}$                                  | -   | 1.9 | -   |               |
| $Q_{gd}$  | Gate-drain charge            | (see Figure 13. Gate charge test circuit)                             | -   | 2.1 | -   |               |

**Table 5. Switching times**

| Symbol       | Parameter           | Test conditions  | Min | Typ  | Max | Unit |
|--------------|---------------------|--|-----|------|-----|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = -15\text{ V}$ , $I_D = -2\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = -10\text{ V}$<br>(see Figure 12. Switching times test circuit for resistive load) | -   | 5.4  | -   | ns   |
| $t_r$        | Rise time           |  | -   | 5    | -   |      |
| $t_{d(off)}$ | Turn-off delay time |  | -   | 19.2 | -   |      |
| $t_f$        | Fall time           |  | -   | 3.4  | -   |      |

**Table 6. Source drain diode**

| Symbol                  | Parameter          | Test conditions                                | Min | Typ | Max  | Unit |
|-------------------------|--------------------|--|-----|-----|------|------|
| $V_{SD}$ <sup>(1)</sup> | Forward on voltage | $I_{SD} = -2\text{ A}$ , $V_{GS} = 0\text{ V}$ | -   | -   | -1.1 | V    |

| Symbol    | Parameter                | Test conditions   | Min | Typ | Max  | Unit |
|-----------|--------------------------|---|-----|-----|------|------|
| $t_{rr}$  | Reverse recovery time    | $I_{SD} = -2 \text{ A}$ ,<br>$di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 24 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$<br>(see Figure 14. Test circuit for inductive load switching and diode recovery times) | -   | -   | 11.2 | ns   |
| $Q_{rr}$  | Reverse recovery charge  |   | -   | -   | 3.5  | nC   |
| $I_{RRM}$ | Reverse recovery current |   | -   | -   | -0.6 | A    |

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

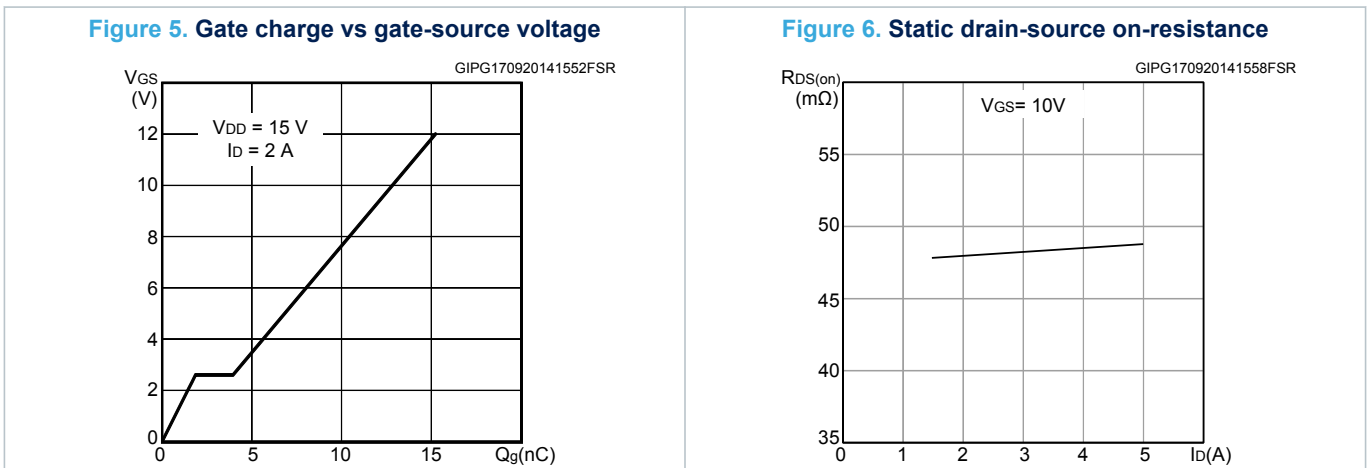
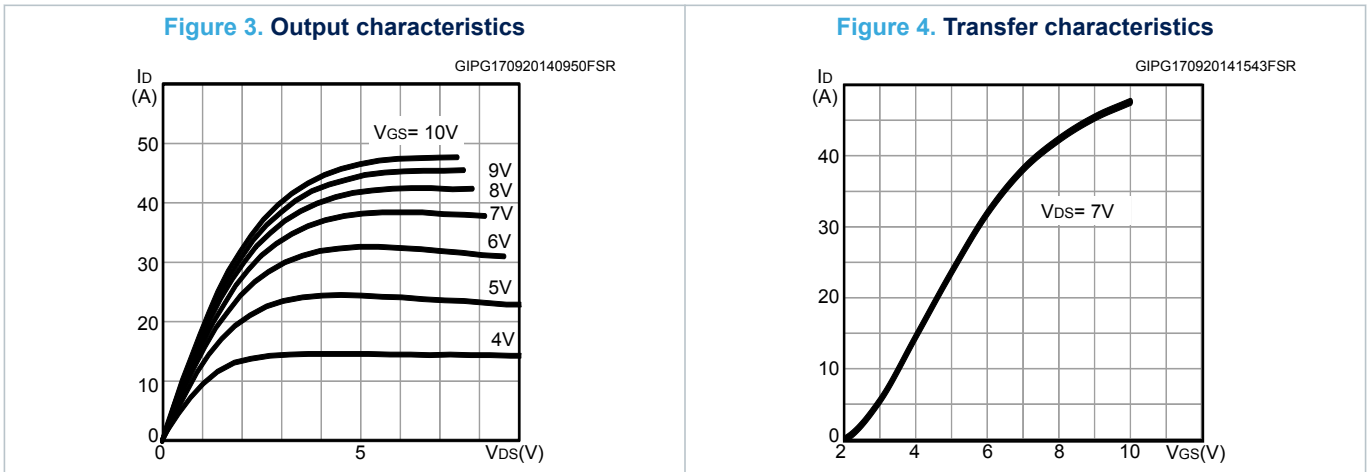
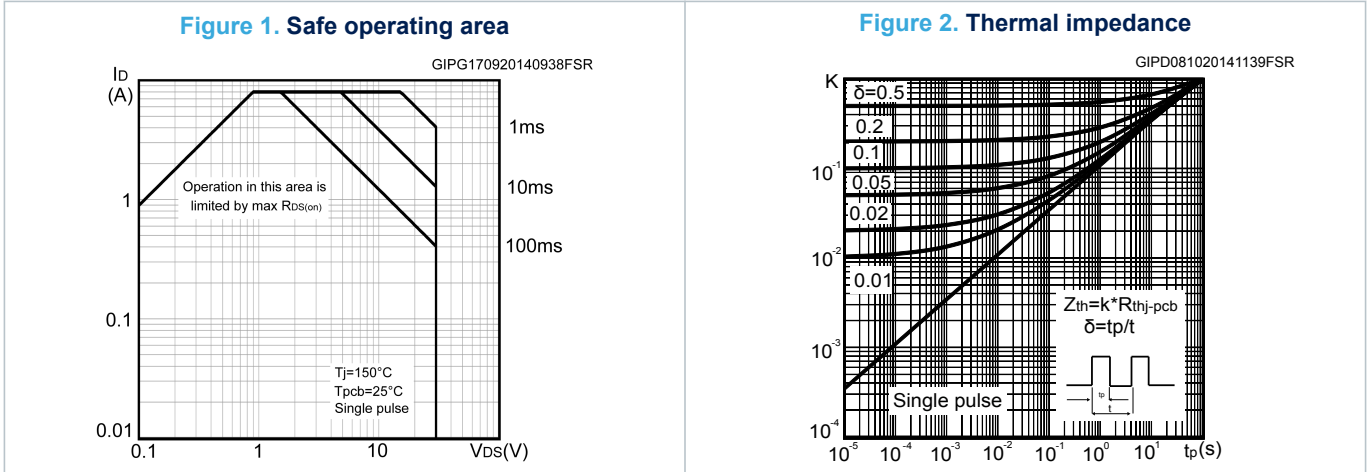


Figure 7. Normalized  $V_{(BR)DSS}$  vs temperature

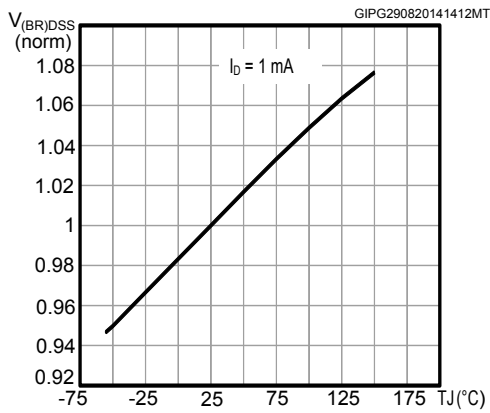


Figure 8. Capacitance variations

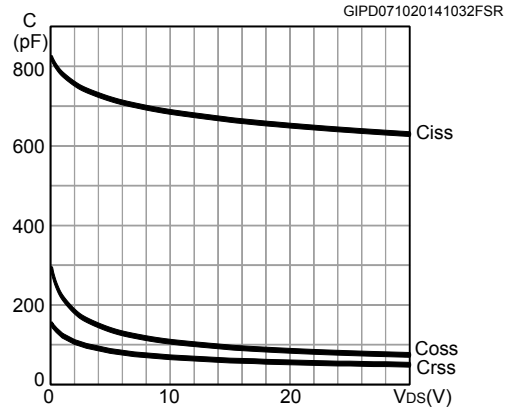


Figure 9. Normalized gate threshold voltage vs. temperature

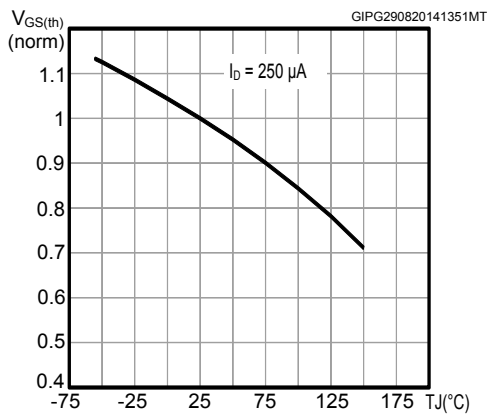


Figure 10. Normalized on-resistance vs. temperature

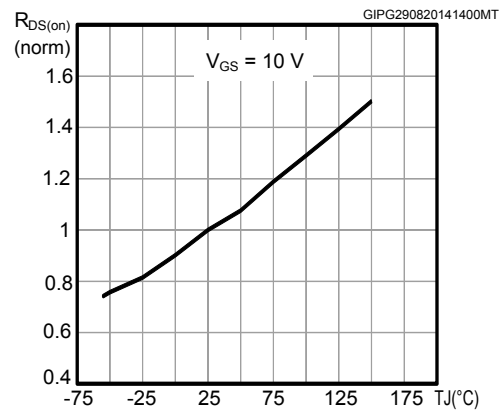
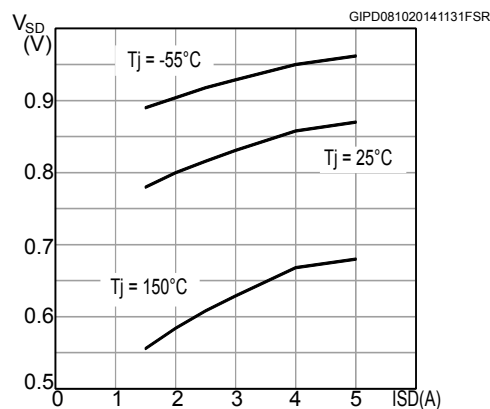
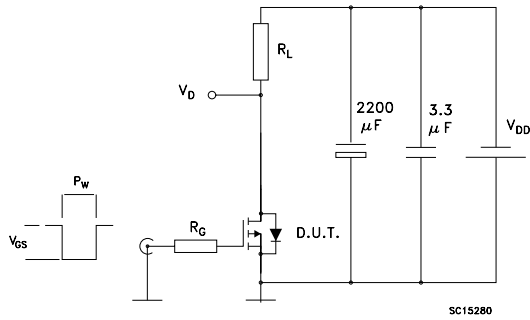
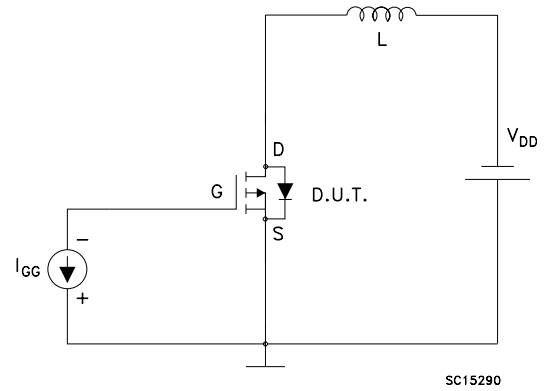
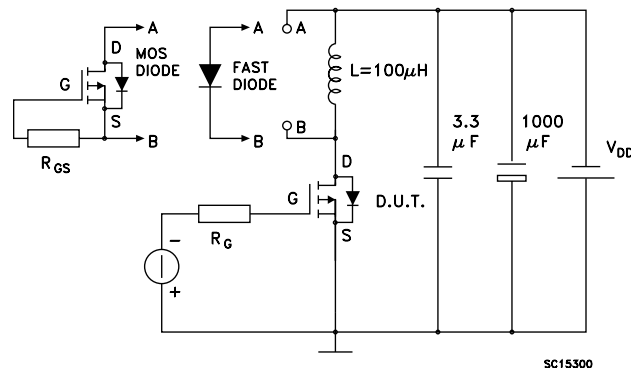


Figure 11. Source-drain diode forward characteristics



### 3 Test circuits

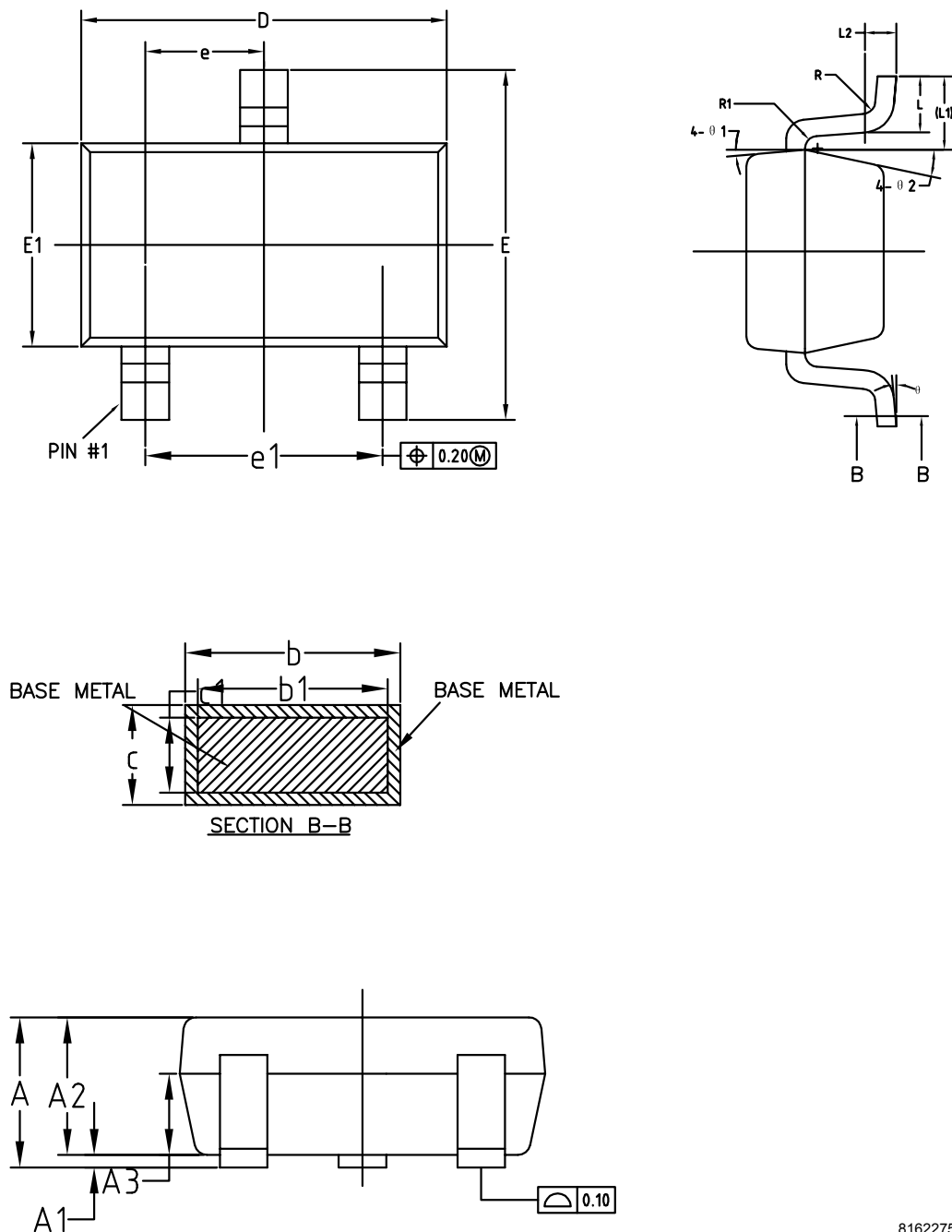
**Figure 12. Switching times test circuit for resistive load**

**Figure 13. Gate charge test circuit**

**Figure 14. Test circuit for inductive load switching and diode recovery times**


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 SOT-23 package information

Figure 15. SOT-23 package outline

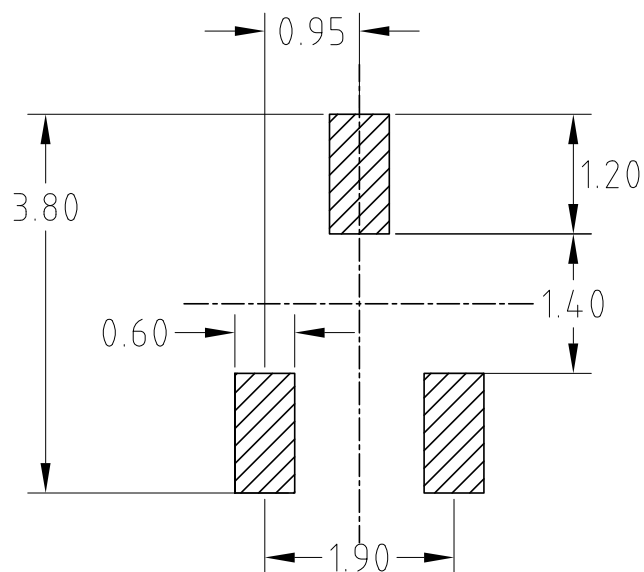


8162275\_998G\_3



**Table 7. SOT-23 package mechanical data**

| Dim.       | mm       |       |       |
|------------|----------|-------|-------|
|            | Min.     | Typ.  | Max.  |
| A          |          |       | 1.25  |
| A1         | 0.00     |       | 0.15  |
| A2         | 1.00     | 1.10  | 1.20  |
| A3         | 0.60     | 0.65  | 0.70  |
| b          | 0.36     |       | 0.50  |
| b1         | 0.36     | 0.38  | 0.45  |
| c          | 0.14     |       | 0.20  |
| c1         | 0.14     | 0.15  | 0.16  |
| D          | 2.826    | 2.926 | 3.026 |
| E          | 2.60     | 2.80  | 3.00  |
| E1         | 1.526    | 1.626 | 1.726 |
| e          | 0.90     | 0.95  | 1.00  |
| e1         | 1.80     | 1.90  | 2.00  |
| L          | 0.35     | 0.45  | 0.60  |
| L1         | 0.59 REF |       |       |
| L2         | 0.25 BSC |       |       |
| R          | 0.05     |       |       |
| R1         | 0.05     |       |       |
| $\theta$   | 0°       |       | 8°    |
| $\theta_1$ | 3°       | 5°    | 7°    |
| $\theta_2$ | 6°       |       | 14°   |

**Figure 16. SOT-23 recommended footprint (dimensions are in mm)**


## Revision history

**Table 8. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 09-May-2013 | 1        | Initial release.   |
| 03-Nov-2014 | 2        | Document status promoted from preliminary to production data.<br>Added Section 2.1: "Electrical characteristics (curves)".<br>Minor text changes.  |
| 05-Nov-2015 | 3        | Updated title and features in cover page.<br>Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> , <i>Table 7: "Source drain diode"</i> and <i>Section 2.1: "Electrical characteristics (curves)"</i> .<br>Minor text changes. |
| 21-Feb-2018 | 4        | Removed maturity status indication from cover page. The document status is production data.<br>Updated <i>Section 4.1 SOT-23 package information</i> .<br>Minor text changes.  |
| 26-Mar-2019 | 5        | Updated <a href="#">Table 3. On /off states</a> .<br>Minor text changes.   |

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