Keywords: high-speed ADC, high-speed analog-to-digital converter, high dynamic performance, RF receiver, Rx, transmitter, Tx, base station systems, BTS, AMPS, CDMA, WCDMA, mixer, IF, dynamic range, AGC, VGA, RF, baseband, signal-to-noise ratio, SNR, blocker, c

APPLICATION NOTE 3062

Dynamic Performance Requirements for High-Performance ADCs and RF Components in Digital Receiver Applications

Jun 15, 2004

Abstract: Today's basestation systems (BTS) have to meet a variety of different standards and must fulfill critical specifications in various blocks of the signal chain. The following paper identifies these demands in signal chain components such as high dynamic performance ADCs, variable gain amplifiers, mixers and local oscillators and details their use in a typical BTS application and how they meet the stringent requirements for high dynamic performance, high intercept performance and low noise.

Click here for an overview of the wireless components used in a typical radio transceiver.

Demanding requirements are placed on high-performance analog-to-digital converters (ADCs) and analog components in most digital receivers. In cellular base station digital receivers for example, sufficient dynamic range is needed to handle high-level interferers (or blockers) while properly demodulating the lower level desired signal. Maxim's MAX1418 15-bit 65Msps or MAX1211 12-bit 65Msps ADC, in combination with the MAX9993 2GHz or MAX9982 900MHz integrated mixers, provide exceptional dynamic range for two of the most critical stages in a receiver line-up. In addition, Maxim's MAX2027 and the MAX2055 IF digital variable gain amplifiers (DVGAs) provide exceptionally high third order output intercept performance (OIP3) with the required gain adjustment range for many applications.

A cellular base station (BTS: Base Transceiver Station) consists of many different hardware modules including one that performs the RF receiver (Rx) and transmitter (Tx) functionality - namely a transceiver (TRx). In the older analog AMPS and TACS BTSs, one transceiver handles a duplexed Rx and Tx RF carrier. Many transceivers are needed to provide enough carriers to obtain the required calling coverage. Analog technology is being replaced by CDMA and WCDMA worldwide, and Europe adapted GSM over a decade ago. In CDMA, many callers utilize the same RF frequency, which allows a single transceiver to handle many callers' signals simultaneously. Various CDMA and GSM designs exist today and methods to reduce cost and power are continuously being sought by BTS manufacturers. Optimizing single-carrier solutions or developing multi-carrier receivers can accomplish this. **Figure 1** illustrates the main blocks in a subsampling receiver architecture commonly used in BTS equipment.

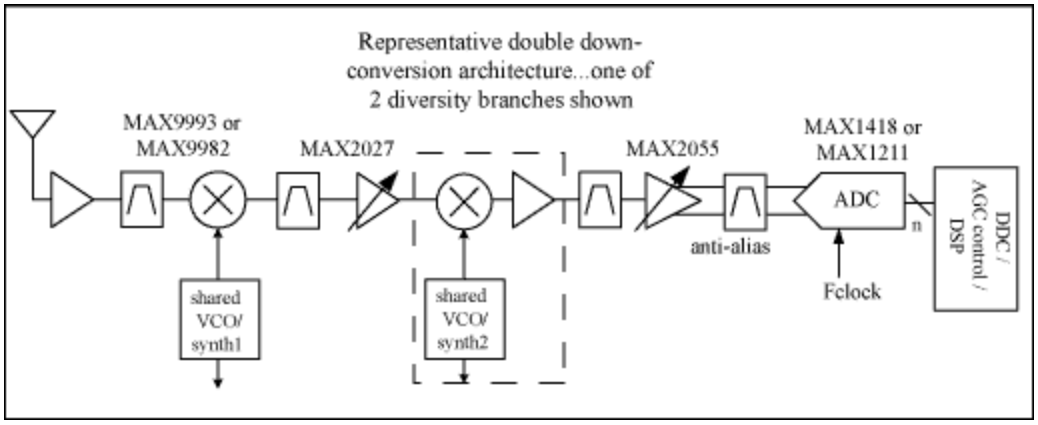

Figure 1. Subsampling receiver architecture.

Maxim's MAX9993 2GHz mixer and MAX9982 900MHz mixer provide the gain and high linearity coupled with low noise figure allowing the designer to eliminate lossy, passive mixers in many designs. The MAX2027 and MAX2055 are designed to operate in the 1st or 2nd IF stages of the receiver. Both offer +40dBm third order output intercept (OIP3) performance over their entire gain adjustment range. Even though the MAX1418 (15-bit 65Msps) and MAX1211 (12-bit 65Msps) data converters are illustrated in Figure 1, other speed grades satisfying most applications are included in both converter families. If the second down conversion is eliminated (shown in dashed lines), the figure depicts a single down conversion architecture.

Maxim's Low Noise ADC, MAX1418

For the subsampling receiver architecture shown in Figure 1, stringent noise and distortion requirements are placed on the ADC. In receiver applications, the lower level desired signal is digitized alone or in the presence of an unwanted signal(s) that can be significantly larger in amplitude. To properly design the receiver, the ADC effective noise figure must be determined under these two signal extremes. The converter's noise figure is determined by comparing its total noise power to the thermal noise floor. For small analog input signals, the thermal + quantization noise power dominate the ADC's noise floor, which is used to approximate the ADC's effective noise figure (NF).

In practice, once the ADC's effective noise figure is known in the small signal condition, and the cascaded noise figure of the analog circuitry (RF & IF) is determined, the minimum power gain ahead of the ADC is selected to meet the required receiver noise figure. The amount of power gain places an upper limit on the maximum blocker, or highest interference level the receiver can tolerate before the ADC overloads. For BTS applications, the ADC often does not have sufficient dynamic range to meet both the noise figure requirements (receiver sensitivity) and maximum blocker requirements without implementing automatic gain control (AGC). The AGC can be included either in the RF stages, IF stages, or both.

Other converters in the MAX1418 family are optimized for baseband performance where $f_{INPUT} = f_{CLOCK/2}$. Operating in this frequency range and using these baseband optimized parts provide the best possible converter dynamic range. These converters include the MAX1419 optimized for a 65Msps clock rate and the MAX1427 optimized for a clock rate of 80Msps, both with SFDR performance equal to 94.5dBc at baseband.

The following example uses the MAX1418 specifications listed in Table 1:

Table 1. MAX1418 Electrical Characteristics

Parameter	Condition	Symbol	Typ Value	Units

Resolution		N	15	Bits
Analog Input Range		VID	2.56	V_{P-P}
Differential Input Resistance		RIN	1	kΩ
AC Specifications	f_{CLK} = 65Msps			
Thermal + Quantization Noise Floor	Analog input = -35dBFS	Nfloor	-78.2	dBFS
Signal-to-Noise Ratio Analog in = -2dBFS	f_{IN} = 70MHz	SNR	73.6	dB
Spurious-Free Dynamic Range Analog in = -2dBFS	f_{IN} = 70MHz	SFDR	84	dB
Signal-to-Noise-and-Distortion Analog in = -2dBFS	f_{IN} = 70MHz	SINAD	73.3	dB

The MAX1418 can be used with a 14-bit interface by not connecting the LSB. If so used, there is a slight SNR performance penalty and the SFDR performance remains essentially unaffected.

Figure 2 illustrates the ADC noise contribution in the absence of a large-level blocker. Assume all the analog circuitry in front of the ADC has a cascaded noise figure of 3.5dB. As a first approximation, suppose a designer's goal is for the ADC to degrade the overall receiver noise figure by no more than 0.2dB to meet some target sensitivity in a CDMA base station receiver. This noise figure value should provide sufficient margin to the air-interface requirements, which is also dependent on the final detector's Eb/No (bit energy to noise power spectral density ratio) requirement. If the MAX1418 Thermal + Quantization Noise Floor value from Table 1 is used, an equivalent noise figure of 26.9dB can be calculated when the device is clocked at 61.44Msps (50x chip rate). The ADC noise in the 1.23MHz CDMA channel bandwidth is 14dB lower than the noise in the Nyquist bandwidth due to the processing gain achieved. An overall gain of 36dB is needed to achieve the desired cascaded receiver noise figure value of 3.7dB.

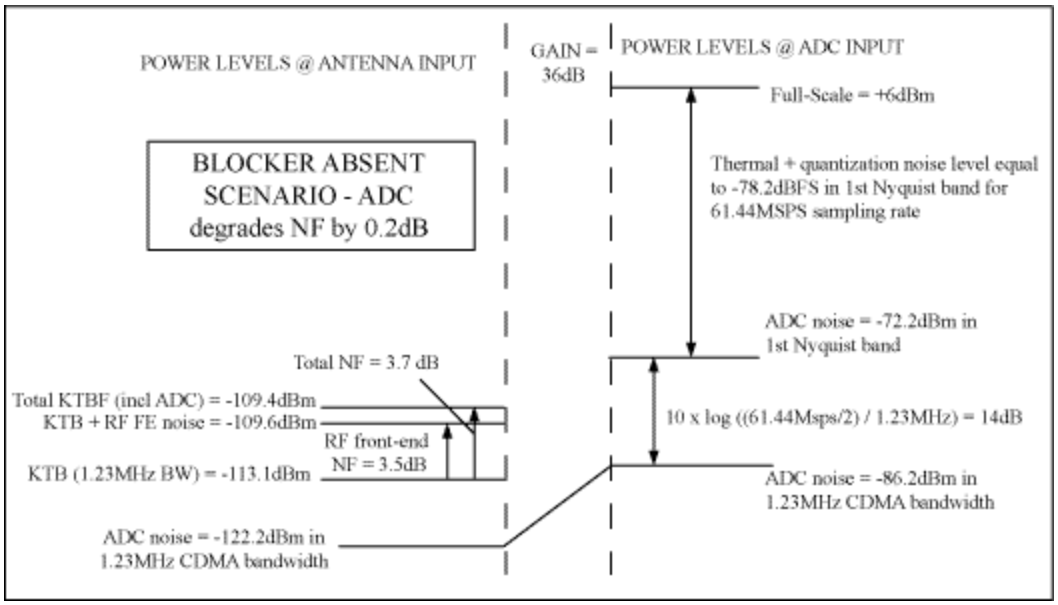

Figure 2. ADC noise contribution for no blocker.

With 36dB gain ahead of the ADC, a maximum single tone blocker level above -30dBm at the antenna terminal will exceed the ADC full-scale input. The cdma2000® cellular base station standard specifies a maximum allowable blocker level of -30dBm at the antenna terminal. For this example, 6dB gain reduction is used to increase the largest allowable blocker signal applied to the ADC providing margin to

the standard's specification. Assuming 2dB headroom is allowed, 6dB gain reduction results in a maximum blocker level of -26dBm at the antenna and +4dBm at the ADC input (see **Figure 3**). The cellular standards allow 3dB degradation in overall (noise + distortion) relative to reference sensitivity when a single-tone blocker is present. The allocation of individual noise and distortion components is left up to the designer.

Suppose the designer allows the RF front-end cascaded noise plus distortion to degrade the NF by 1dB (from the nominal 3.5dB) when the blocker is present with 6dB of AGC applied. With only 30dB of gain in front of the ADC and an effective noise figure of 29.4dB determined by the ADC SNR performance, the cascaded receiver noise figure is 5.7dB in the 'blocked condition', which is a 2dB degradation from 3.7dB noise figure calculated for receiver sensitivity. Because this calculation does not take into account the spurious performance, an additional 1dB degradation can be allowed for the ADC's spurious free dynamic range (SFDR) performance. Instead of calculating noise and SFDR contributions separately, SINAD could have been used to compute the effective NF when a blocker signal is present.

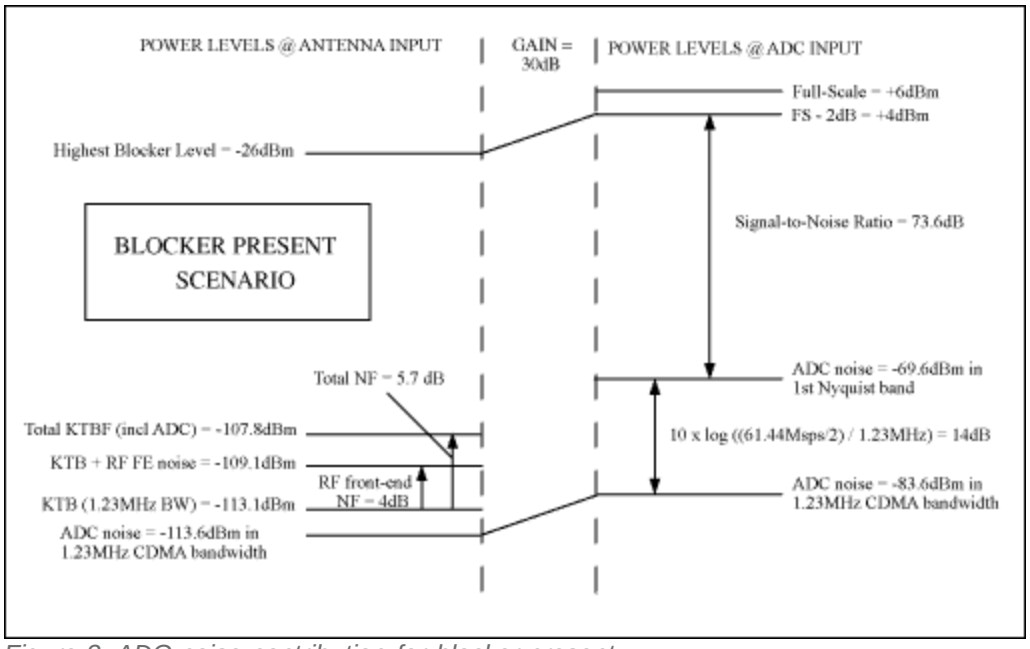

Figure 3. ADC noise contribution for blocker present.

MAX1211 Allows Single Down Conversion Architecture

The subsampling architecture can be used with a single down conversion architecture if sufficient SNR & SFDR performance can be obtained from the converter at higher IF frequencies. Maxim's MAX1211 is a 12-bit 65Msps converter designed with this architecture in mind along with pin-compatible 80Msps and 95Msps versions that will soon be released. This family of converters allows direct IF sampling for input frequencies up to 400MHz along with advanced features such as differential or single-ended clock input, allows 20% to 80% clock duty cycle, data valid indicator allowing the simplification of clock and data timing, 2's complement or gray code digital output data format all in a small 40-pin thin QFN package (6mm x 6mm x 0.8mm). See Table 2 for the typical MAX1211 AC specifications illustrating the superb AC performance for an analog input frequency of 175MHz. (Note: An improved MAX1211 version, whose AC specifications are given in the table below, will be available in about one month.)

Table 2. MAX1211 Electrical Characteristics

Parameter	Condition	Symbol	Typ Value	Units

Resolution		N	12	Bits
Analog Input Range		VID	2	V_{P-P}
Differential Input Resistance		RIN	15	kΩ
AC Specifications	f_{CLK} = 65Msps			
Thermal + Quantization Noise Floor	Analog input = -35dBFS	Nfloor	69.3	dBFS
Signal-to-Noise Ratio Analog in = -0.2dBFS	f_{IN} = 32.5MHz f_{IN} = 175MHz	SNR	68.3 66.8	dB
Spurious-Free Dynamic Range Analog in = -0.2dBFS	f_{IN} = 32.5MHz f_{IN} = 175MHz	SFDR	82.4 79.7	dB
Signal-to-Noise-and-Distortion Analog in = -2dBFS	f_{IN} = 32.5MHz f_{IN} = 175MHz	SINAD	68.1 66.5	dB

There are significant advantages gained when choosing single down conversion instead of double down conversion. By eliminating the second down conversion mixer, second-IF gain stages, and 2nd LO synthesizer circuitry, the parts count and board space can be reduced by approximately 10% and cost by $10 to $20.

Spurious Considerations for Different Architectures

If saving parts count, board space, power, and cost don't provide enough incentive, the following example illustrates the frequency planning advantage gained when using the MAX1211 in a single down conversion architecture. Suppose a cdma2000 receiver is designed to operate in the PCS frequency band. For a sample rate of 61.44Msps and synthesizer reference frequency of 30.72MHz, choose a first IF frequency centered in the sixth Nyquist band at 169MHz having a bandwidth of approximately 1.24MHz. Using the same first IF center frequency of 169MHz, the DDC architecture assumes a 2nd IF frequency is centered in the 2nd Nyquist band at 46.08MHz.

Table 3. Spur Search Assumptions for SDC & DDC Architectures

SDC	DDC	Parameter	Value
x	x	Receive band	1904.3800 to 1905.6200MHz
x	x	Clock Frequency	61.44000MHz
x	x	Max clock harmonic	30
x	x	Synthesizer ref freq	30.7200MHz
x	x	Max synthesizer harmonic	40
x	x	First injection LS	1736.0000MHz
x	x	Max 1st LO harmonic	5
x	x	Receive image band	1566.3800 to 1567.6200MHz
x	x	First IF band	168.3800 to 169.6200MHz
	x	Second injection LS	122.9200MHz
	x	Max 2nd LO harmonic	5
	x	1st IF image band	76.2200 to 77.4600MHz
	x	Second IF band	45.4600 to 46.7000MHz

Table 3 lists the spur search assumptions for an RF carrier near the upper end of the PCS band for the

single-carrier, single down conversion (SDC) and double down conversion (DDC) architectures. For the SDC architecture, the spur search resulted in 134 total spurs in the RF receive band, receive image band, IF band, and IF image band. Most of these spurs are high order and will not degrade the receiver's performance. For the DDC architecture, this spur search results in over 2400 spurs, which 18 times more than what was calculated for the SDC architecture. These spurious products occur in the RF receive band, receive image band, 1^{st} IF band, 1^{st} IF image band, 2^{nd} IF band, and 2^{nd} IF image band. The spurs resulting from combinations of higher clock harmonics and synthesizer reference frequency will be relatively easy to reduce through good board layout practices and filtering. However, a significant number of lower order spurs will be difficult to minimize.

Maxim's IF Amplifiers, MAX2027 & MAX2055

Maxim also offers high performance IF amplifiers having digital variable gain control in 1dB increments. The MAX2027 is a digital variable gain amplifier (DVGA) having single-ended input / single-ended output for frequencies ranging from 50MHz to 400MHz. This DVGA offers a low noise figure of 5dB at maximum gain. The MAX2055 is a single-ended input / differential output DVGA meant to drive high-performance ADCs for frequencies ranging from 30MHz to 300MHz. A step-up transformer can be used between the differential output of the MAX2055 and the ADC differential input. The transformer is driven differentially; thus optimizing the transformer performance and balance between the output signals. Both DVGAs operate from 5V bias and have +40dBm OIP3 over all gain setting ranges. See the associated data sheets on Maxim's web site for additional detail at www.maximintegrated.com.

Maxim's High Linearity Mixers, MAX9993 & MAX9982

In receiver circuits, mixers are subjected to large input signals that place stringent requirements on their performance. Ideally, the mixer output signal amplitude and phase are proportional to the input signal's amplitude and phase and independent of the LO signal characteristics. Using this assumption, the amplitude response of the mixer is linear for the RF input and is independent of the LO input.

However, mixer nonlinearities produce undesired mixing products called spurious responses, which are caused by undesired signals reaching the mixer's RF input port and producing a response at the IF frequency. When they interfere with the desired IF frequency, the mixing mechanism can be described by:

$f_{IF} = \pm mf_{RF} \pm nf_{LO}$ where IF, RF, and LO refer to the signals at designated ports respectively and m and n are integer harmonics of both the RF and LO frequencies that mix to create numerous combinations of spurious products.

Integrated (or active) balanced mixer designs, such as Maxim's MAX9993 and MAX9982 are becoming more popular as their performance rivals that of passive mixer solutions. Balanced mixers reject certain spurious responses when m or n is even resulting in excellent 2^{nd} order harmonic performance. Ideal double balanced mixers reject all responses where m or n (or both) is even. The IF, RF, and LO ports are mutually isolated in all double balanced mixers. With properly designed baluns, these mixers can have overlapping RF, IF, and LO bands. The MAX9993 and MAX9982 features include: gain, low noise figure, integrated LO buffer, low LO drive, LO switch allowing two LO frequency inputs, superb LO noise performance, and integrated RF baluns on the RF and LO ports.

Maxim's mixers have built-in LO buffers with superb LO noise performance that ease the input LO power requirements driving them. LO noise reciprocally mixes with high-level input blocking signals that desensitize the receiver. Both MAX9993 and MAX9982 have low noise LO buffers designed to have minimal impact on receiver desensitization when blockers are present. For example, suppose the VCO providing the injection signal has a sideband noise performance of -145dBc/Hz. The typical LO noise performance for the MAX9993 is -164dBc/Hz so the composite sideband noise performance is degraded

by only 0.05dBc/Hz to -144.95dBc/Hz. This way, the user not only benefits from needing to provide a low-level LO injection signal to the mixer, but can also be assured the reciprocal mixing performance of the receiver is not degraded due to the MAX9993 LO buffer performance.

A particularly troublesome 2nd order spurious response called the half-IF (1/2 IF) spurious response is defined for the mixer indices of (m = 2, n = -2) for low-side injection and (m = -2, n = 2) for high-side injection. For low-side injection, the input frequency that creates the half-IF spurious response is located below the desired RF frequency by an amount $f_{IF}/2$ from the desired RF input frequency (see **Figure 4**). The desired RF frequency is represented by 1909MHz, and in combination with the LO frequency of 1740MHz, the resulting IF frequency is 169MHz. Though the CDMA RF and IF carrier occupies a 1.24MHz bandwidth, it's illustrated as a single frequency indicating the center carrier frequency. For this example, the undesired signal at 1824.5MHz causes a half-IF spurious product at 169MHz.

Verify:
$2 \times f_{Half\text{-}IF} - 2 \times f_{LO} =$
$2 \times (f_{RF} - f_{IF}/2) - 2 \times (f_{RF} - f_{IF}) =$
$2 \times (f_{RF} - 2 \times f_{IF}/2) - 2 \times f_{RF} + 2 \times f_{IF} = f_{IF}$

Results in:
2 x 1824.5MHz - 2 x 1740MHz = 169MHz

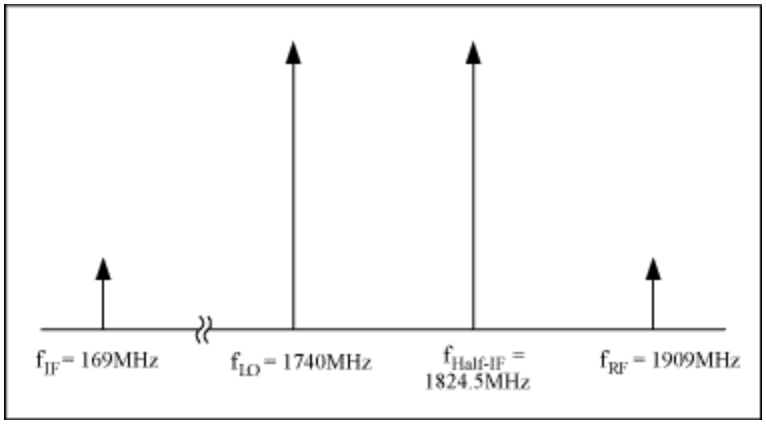

Figure 4. Frequency locations for desired f_{RF}, f_{LO}, f_{IF}, and undesired $f_{Half\text{-}IF}$.

The amount of rejection, called the 2x2 spurious response, can be predicted from the mixer's second order intercept point, IP2. The 2x2 IMR or spurious values in **Figure 5** are taken from Maxim's MAX9993 data sheet. Note the signal levels in the figure are referred to the input of the mixer for which the input IP2 (IIP2) performance is calculated.

Such superb level of 2x2 performance results in the following:

$IIP2 = 2 \times IMR + P_{SPUR} = IMR + P_{RF}$
$= 2 \times 70dBc + (-75dBm) = 70dBc + (-5dBm)$
$= +65dBm$

Similarly, Maxim's MAX9982 900 MHz active mixer provides typical 2RF - 2LO spurious response equal to 65dBc under similar conditions which results in:

$IIP2 = 2 \times IMR + P_{SPUR} = IMR + P_{RF}$
$= 2 \times 65dBc + (-70dBm) = 65dBc + (-5dBm)$

= +60dBm

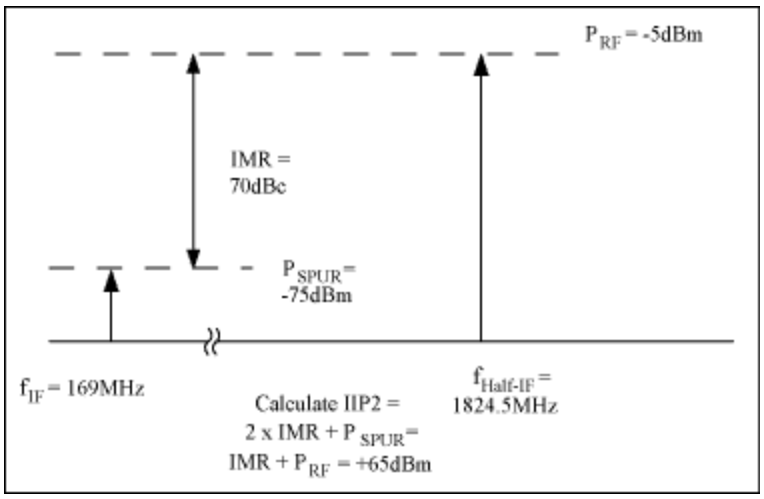

Figure 5. 2nd -order intercept calculation for signals referred to mixer input, IIP2.

Image-reject filters used in the RF path immediately ahead of the mixer attenuate any amplifier harmonics. The noise filter in the LO path attenuates harmonics caused by the LO injection source. High-level input signals create distortion or intermodulation products and can be quantified by calculating the intercept point, either at the input or output of the device or system. For the case where the mixer LO power is held constant, the order of the intercept point or distortion product is determined only by the RF multiplier and not by the LO multiplier because variations in the RF signal are only of concern. The order refers to how fast the amplitudes of the distortion products increase with a rise in input level.

It's been shown that Maxim's MAX1418 15-bit ADC offers excellent noise performance resulting in low required receiver gain thus withstanding higher blocker or interference levels with minimum AGC. The MAX1211 ADC family is ideally suited for a single-conversion receiver architecture with 1st IF input frequencies up to 400MHz. In addition, Maxim's RF MAX9993 and MAX9982 mixers provide the desired linearity along with low noise figure and sufficient power gain to eliminate the need for passive mixers in many of today's receiver designs. Maxim's MAX2027 and MAX2055 DVGAs provide a typical OIP3 value of approximately +40dBm over their entire gain adjustment range. Taken together, a receiver lineup incorporating these components can achieve a high level of performance in a very cost effective solution.

1. The output intercept point is merely the input intercept point plus the gain (in dB) of the circuit or system under measurement.

References

1. Referenced application notes found on Maxim's web site www.maximintegrated.com include:
   - AN 728 'Defining and Testing Dynamic Parameters in High-Speed ADCs, Part 1'
   - AN 729 'Dynamic Testing of High-Speed ADCs, Part 2'
   - AN 1197 'How Quantization and Thermal Noise Determine an ADC's Effective Noise Figure'
   - AN1929 'Understanding ADC Noise for Small and Large Signal Inputs for Receiver Applications'
   - AN 1838 'Mixer 2x2 Spurious Response and IP2 Relationship'
   - AN 2021 'Specifications and Measurement of Local Oscillator Noise in Integrated Circuit Base Station Mixers'
   - AN 2371 'Consider Overall Cascaded Performance When Comparing Integrated RF Frequency Mixers to Passive Mixer Solutions'
2. 'Digital Techniques for Wideband Receivers' by James Tsui, Artech House Publishers, 1995.

3. 'RF Design Guide, Systems, Circuits, and Equations' by Peter Vizmuller, Artech House Publishers, 1995
4. 'CDMA Systems Engineering Handbook' by Jhong Sam Lee & Leonard E. Miller, Artech House Publishers, 1998.

A similar version of this article appeared in the February issue of *Microwaves&RF* magazine.

Related Parts		
MAX1211	12-Bit, 65Msps, IF Sampling ADC	
MAX1418	15-Bit, 65Msps ADC with -78.2dBFS Noise Floor for IF Applications	
MAX2027	IF Digitally Controlled Variable-Gain Amplifier	
MAX2055	Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier	
MAX9982	825MHz to 915MHz, SiGe High-Linearity Active Mixer	Free Samples
MAX9993	High-Linearity 1700MHz to 2200MHz Down-Conversion Mixer with LO Buffer/Switch	Free Samples

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