

PCN Number:	20190219002.0.A	PCN Date:	July 2, 2019
Title:	Datasheet for TPS659038-Q1, TPS659039-Q1		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



TPS659038-Q1, TPS659039-Q1

SWCS095K – AUGUST 2013 – REVISED JANUARY 2018

Changes from Revision J (March 2017) to Revision K

Page

• Removed pullup and pulldown from BOOT0 pin description	16
• Deleted the nominal T_{stg} value (27°C) from the <i>Absolute Maximum Ratings</i> table	18
• Deleted the voltage mode to the I/O digital supply voltage, VIO_IN parameter from the <i>Recommended Operating Conditions</i> table	19
• Deleted the voltage on the VCC1 GPADC pins (TBC) parameter from the <i>Recommended Operating Conditions</i> table	19
• Added 2-A mode for SMPS6 in the test conditions for high-side and low-side MOSFET forward current limit and low-side MOSFET negative current limit in the <i>Electrical Characteristics: Stand-Alone Regulators (SMPS3, SMPS6, SMPS7, SMPS8, and SMPS9)</i> table	24
• Added the number of active SMPS phases (K) to the equation for the temperature compensated result in the <i>Current Monitoring and Short Circuit Detection</i> section	43
• Added additional description of SMPS short detection and recovery behavior	43
• Added equation to convert GPADC code to internal die temperature	52
• Added description of VIO power-up timing, and updated start up timing diagram	73
• Added additional description of VSYS_LO functionality	79
• Added link to application note about POR generation	81



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SWCS095L – AUGUST 2013 – REVISED FEBRUARY 2019

Changes from Revision K (January 2018) to Revision L

Page

• Changed ESD classification from C4B to C3	1
• Updated the LDOVRTC_OUT pulldown resistor recommendation to only include applicable silicon revisions.	11
• Changed ESD Ratings for charge device model on 6 pins	18
• Clarified that LDO1 and LDO2 input pins are not included in this minimum recommended operating voltage. See <i>Electrical Characteristics: LDO Regulators</i> for more information.	19
• Changed minimum recommended operating condition of OSC16MIN from 0V to -0.7V	19
• Added LDO and SMPS output capacitance footnote	20
• Changed VSYS_LO hysteresis from 95mV to 75mV	28
• Updated Caution statement to only include applicable silicon revisions.	37
• Changed discharge resistance to match electrical characteristics table	40
• Added information about shutdown timing during short circuit detection	43
• Updated POWERGOOD description to clarify multi-phase operation.	43
• Updated LDOVRTC note to only include applicable silicon revisions.	48
• Added details on identifying device version	66

• Added typical debounce time from POWERHOLD to the enable of the first rail in the power sequence.	69
• Added VSYS_LO note for applicable silicon revisions.	79
• Updated POR requirements to only include applicable silicon revisions.	81
• SMPS and LDO output capacitance specification further explained	88
• Added design considerations for VCC1 capacitance to support loss of power	88
• Corrected 9-Vpp with 7V absolute maximum specification in the <i>Layout Guidelines</i> section.....	94
• Updated requirements relating to measurement of high-side and low-side FETs in the <i>Layout Guidelines</i> section...	96
• Updated images and description on differential measurements across high-side and low-side FETs	97

The datasheet number will be changing.

Device Family	Change From:	Change To:
TPS659038-Q1, TPS659039-Q1	SWCS095J	SWCS095K
TPS659038-Q1, TPS659039-Q1	SWCS095K	SWCS095L

These changes may be reviewed at the datasheet links provided. If the part number is not listed in the Products Affected section, please contact TI for the customer specific version of the DS.

<http://www.ti.com/product/TPS659039-Q1>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

O9038A342IZWSRQ1	O9038A352IZWSRQ1	O9039A344IZWSRQ1	O9039A360IZWSRQ1
O9039A36BIZWSRQ1	O9039A385IZWSRQ1	O9039A385IZWSTQ1	O9039A387IZWSRQ1
O9039A387IZWSTQ1	O9039A389IZWSRQ1	O9039A389IZWSTQ1	

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