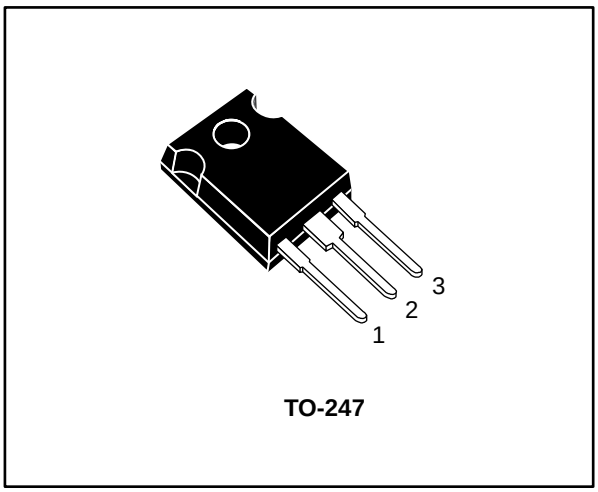
# STW35N60DM2

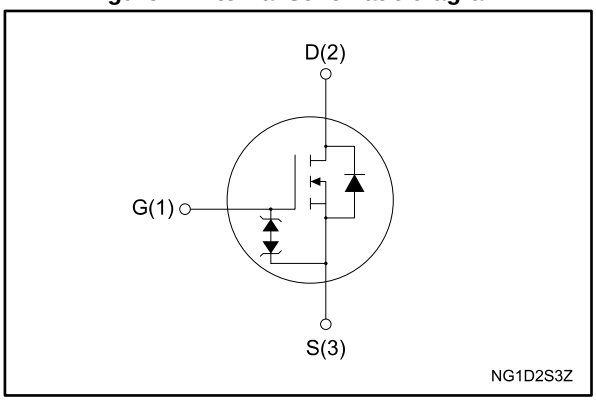
## N-channel 600 V, 0.094 Ω typ., 28 A MDmesh™ DM2 Power MOSFET in a TO-247 package

Datasheet - production data




**TO-247**

**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STW35N60DM2 | 600 V | 0.110 Ω | 28 A | 210 W |

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

## Applications

- Switching applications

## Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge ($Q_{rr}$) and time ($t_{rr}$) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

**Table 1: Device summary**

| Order code | Marking | Package | Packing |
|---|---|---|---|
| STW35N60DM2 | 35N60DM2 | TO-247 | Tube |

# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_{case}$ = 25 °C | 28 | A |
| | Drain current (continuous) at $T_{case}$ = 100 °C | 17 | |
| $I_{DM}$ (1) | Drain current (pulsed) | 112 | A |
| $P_{TOT}$ | Total dissipation at $T_{case}$ = 25 °C | 210 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 50 | V/ns |
| dv/dt (3) | MOSFET dv/dt ruggedness | 50 | |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |
| $T_j$ | Operating junction temperature | | |

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) $I_{SD} \leq 28$ A, di/dt=900 A/µs; $V_{DS}$ peak < $V_{(BR)DSS}$,$V_{DD}$ = 400 V

(3) $V_{DS} \leq 480$ V.

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.6 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-amb | 50 | |

**Table 4: Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive | 6 | A |
| $E_{AS}$ (1) | Single pulse avalanche energy | 650 | mJ |

**Notes:**

(1) starting $T_j$ = 25 °C, $I_D = I_{AR}$, $V_{DD}$ = 50 V.

# 2 Electrical characteristics

($T_{case}$ = 25 °C unless otherwise specified)

**Table 5: Static**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 600 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V | | | 10 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V, $T_{case}$ = 125 °C | | | 100 | |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±25 V | | | ±5 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 14 A | | 0.094 | 0.11 | Ω |

**Table 6: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 2400 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 110 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.8 | - | |
| $C_{oss\ eq.}$ (1) | Equivalent output capacitance | $V_{DS}$ = 0 to 480 V, $V_{GS}$ = 0 V | - | 190 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 A | - | 4.3 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 28 A, $V_{GS}$ = 10 V (see *Figure 15: "Test circuit for gate charge behavior"*) | - | 54 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 14.6 | - | |
| $Q_{gd}$ | Gate-drain charge | | - | 24.2 | - | |

**Notes:**

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.

**Table 7: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 14 A $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*) | - | 21.2 | - | ns |
| $t_r$ | Rise time | | - | 17 | - | |
| $t_{d(off)}$ | Turn-off delay time | | - | 68 | - | |
| $t_f$ | Fall time | | - | 10.7 | - | |

**Table 8: Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 28 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 112 | A |
| $V_{SD}$ (2) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 28 A | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 28 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*) | - | 120 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 572 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 10.2 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 28 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_j$ = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*) | - | 215 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 1.89 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 17.7 | | A |

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

**Table 9: Gate-source Zener diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS}$ = ±250 µA, $I_D$ = 0 A | ±30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.2 Electrical characteristics (curves)

**Figure 2: Safe operating area**

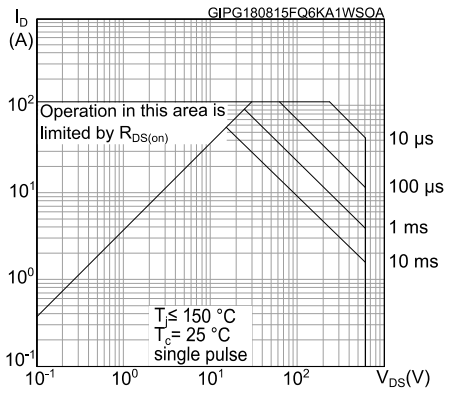



**Figure 3: Thermal impedance**

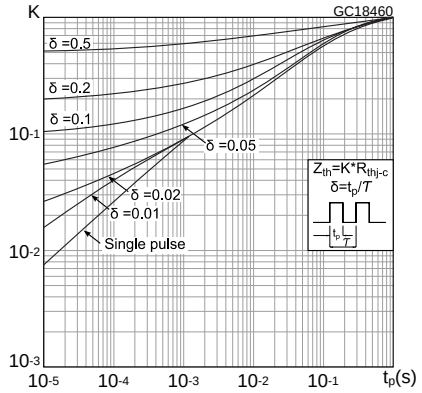



**Figure 4: Output characteristics**

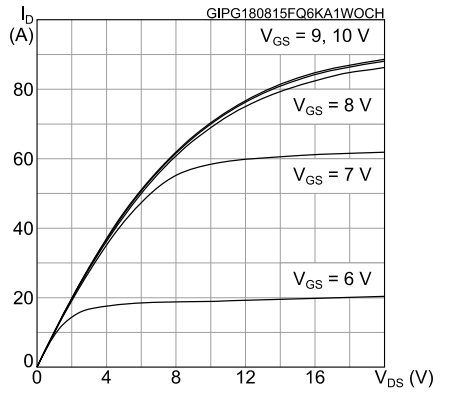



**Figure 5: Transfer characteristics**

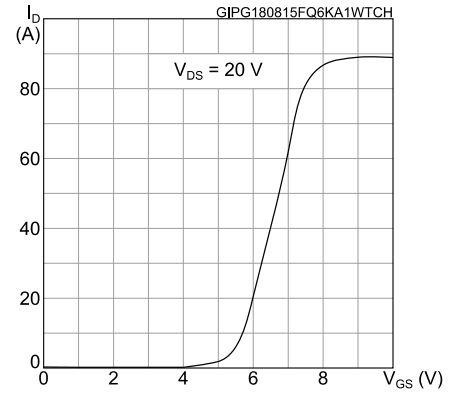



**Figure 6: Gate charge vs gate-source voltage**

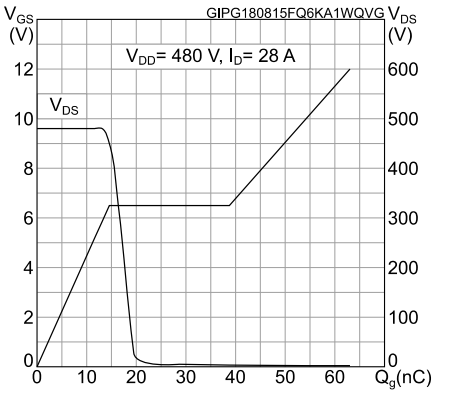



**Figure 7: Static drain-source on-resistance**

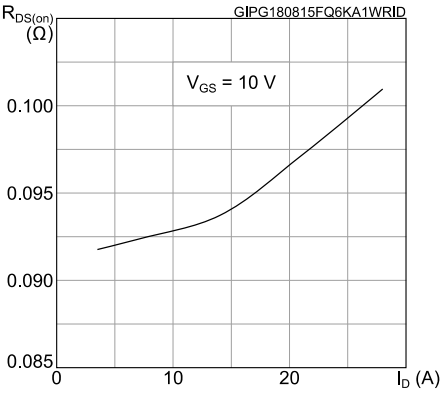


**Figure 8: Capacitance variations**

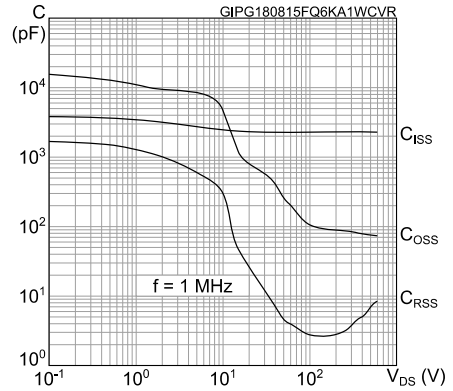



**Figure 9: Normalized gate threshold voltage vs temperature**

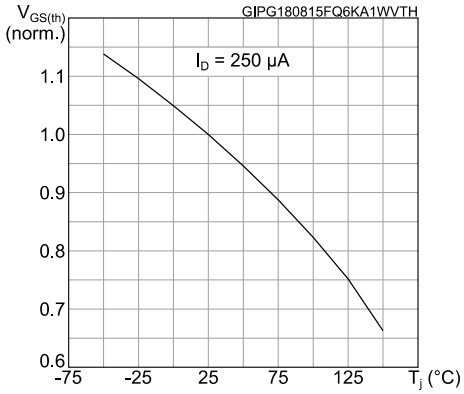



**Figure 10: Normalized on-resistance vs temperature**

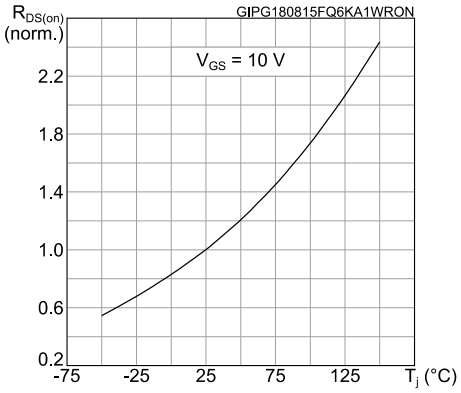



**Figure 11: Normalized V(BR)DSS vs temperature**

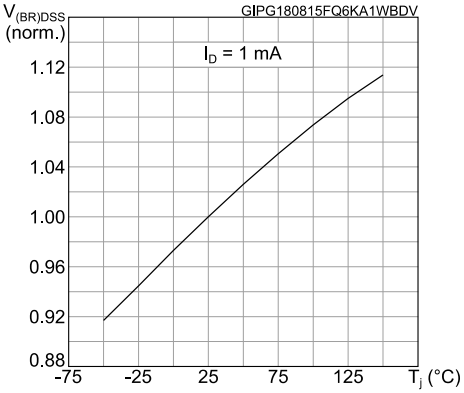



**Figure 12: Output capacitance stored energy**

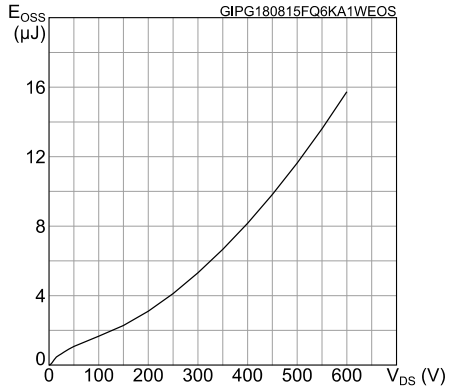
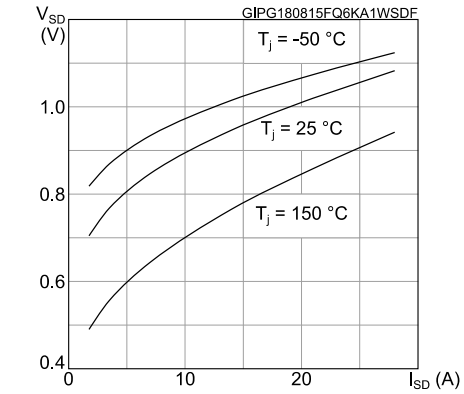



**Figure 13: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**

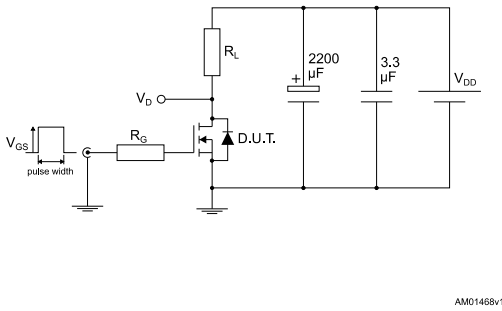



**Figure 15: Test circuit for gate charge behavior**

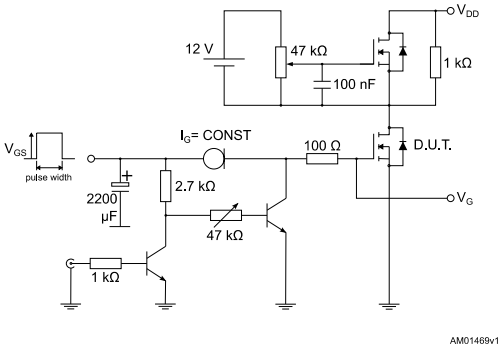



**Figure 16: Test circuit for inductive load switching and diode recovery times**

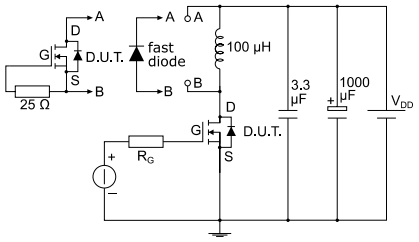



**Figure 17: Unclamped inductive load test circuit**

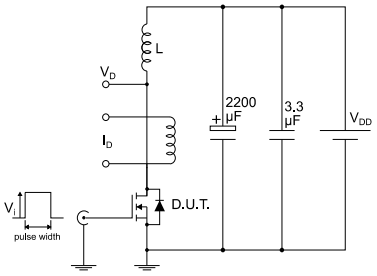



**Figure 18: Unclamped inductive waveform**

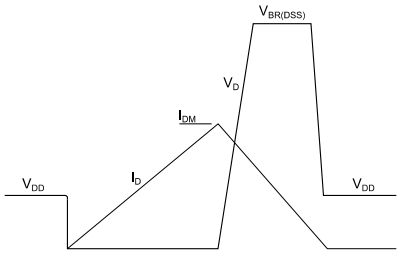
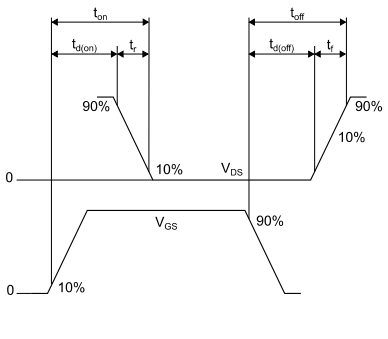



**Figure 19: Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 TO-247 package information

**Figure 20: TO-247 package outline**

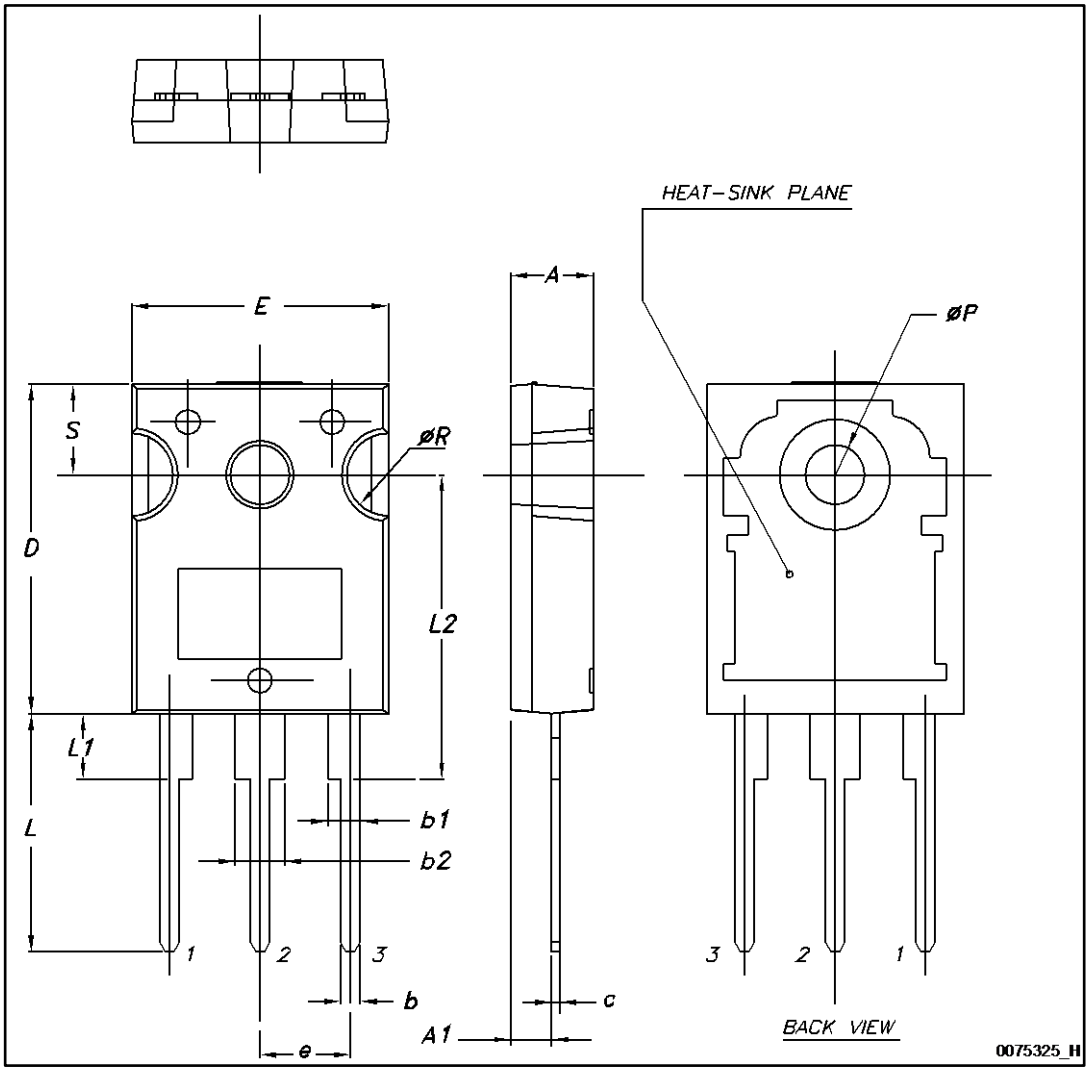


Table 10: TO-247 package mechanical data

| Dim. | mm. | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.85 | | 5.15 |
| A1 | 2.20 | | 2.60 |
| b | 1.0 | | 1.40 |
| b1 | 2.0 | | 2.40 |
| b2 | 3.0 | | 3.40 |
| c | 0.40 | | 0.80 |
| D | 19.85 | | 20.15 |
| E | 15.45 | | 15.75 |
| e | 5.30 | 5.45 | 5.60 |
| L | 14.20 | | 14.80 |
| L1 | 3.70 | | 4.30 |
| L2 | | 18.50 | |
| ØP | 3.55 | | 3.65 |
| ØR | 4.50 | | 5.50 |
| S | 5.30 | 5.50 | 5.70 |

# 5 Revision history

Table 11: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 02-Sep-2015 | 1 | Initial version |

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