

PCN Number:	20200203002	PCN Date:	Mar. 4, 2020
Title:	Datasheet for DP83867CS, DP83867IS, DP83867E		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
		<input type="checkbox"/>	Wafer Bump Site
		<input type="checkbox"/>	Wafer Bump Material
		<input type="checkbox"/>	Wafer Bump Process
		<input type="checkbox"/>	Wafer Fab Site
		<input type="checkbox"/>	Wafer Fab Materials
		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



DP83867CS, DP83867IS, DP83867E

SNLS504C – OCTOBER 2015 – REVISED DECEMBER 2019

Changes from Revision B (March 2017) to Revision C	Page
• Added "Time Sensitive Network (TSN) Compliant" to Features	1
• Changed "Fast Link up / Link Drop Modes" to "Fast Link Drop Mode" in Features	1
• Added "Field Bus Support" to Applications	1
• Deleted "NOTE: Internal pullup and pulldown resistors on the IO pins are disabled when the device enters functional mode after power up." from Pin Functions	6
• Added XI pin voltage ratings to Absolute Maximum Ratings	9
• Added XI Input Voltage section to Electrical Characteristics	10
• Added SGMII Latency nominal values to SGMII Timing ⁽⁴⁾	12
• Changed links to RGMII timing diagrams in RGMII Timing ⁽⁵⁾	12
• Changed T _{holdR} parameter description in RGMII Timing ⁽⁵⁾	13
• Added table note explaining how Duty Cycle % must be interpreted in RGMII Timing ⁽⁵⁾	13
• Added table note explaining how Duty Cycle % must be interpreted in RGMII Timing ⁽⁵⁾	13
• Changed suggestion to program '10M_SGMII_RATE_ADAPT' bit in Serial GMII (SGMII)	24
• Changed statement about PHY address in Serial Management Interface	27
• Deleted mentions of pin strapping to configure Auto-MDIX in Auto-MDIX Resolution	32
• Added Figure 19	32
• Deleted "The BIST allows full control of the packet lengths and of the IPG." from BIST Configuration	33
• Deleted mention of ALCD from Cable Diagnostics	34
• Deleted subsection describing ALCD from Cable Diagnostics	34
• Changed all mentions of "Fast Link Down" to "Fast Link Drop" in Fast Link Drop (FLD)	35
• Added statement on disabling and re-enabling FLD in Fast Link Drop (FLD)	35
• Added sentence about the polarity of MDI signals in Mirror Mode	36

• Changed note after Table 6 to be a table note referenced within the table.	38
• Changed 'MMD3_PCS_CTRL' address to 'MMD3' register 0x0000 in PCS Restart	43
• Deleted mention of MMD7 in PCS Restart.....	43
• Added definition for register Bit Name type 'Strap' in Register Maps	44
• Deleted Advanced Link Cable Diagnostics Control Register (ALCD_CTRL)	44
• Added PAP package default for '1000BASE-T FULL DUPLEX' in 1000BASE-T Configuration Register (CFG1)	54
• Changed 'SGMII_EN' default in PHY Control Register (PHYCR)	57
• Changed 'MDI_CROSSOVER' default in PHY Control Register (PHYCR)	57
• Added PAP package default for 'SPEED_OPT_EN' in Configuration Register 2 (CFG2)	64
• Added Robust Auto MDIX Timer Configuration Register (AMDIX_TMR_CFG).....	73
• Changed descriptions of bits 'FORCE_DROP' and 'FLD_EN' in Fast Link Drop Configuration Register (FLD_CFG)	74
• Added Fast Link Drop Threshold Configuration Register (FLD_THR_CFG).....	75
• Added 'INT_TST_MODE_1' to Configuration Register 4 (CFG4)	75
• Changed 'PORT_MIRROR_EN' default in Configuration Register 4 (CFG4)	75
• Added PAP package default for 'RGMII_EN' in RGMII Control Register (RGMIICTL)	75
• Added Viterbi Module Configuration (VTM_CFG)	78
• Changed description of 'STRAP_FLD' from "Fast Link Detect" to "Fast Link Drop" in Strap Configuration Status Register 2 (STRAP_STS2).....	80
• Added BIST Control and Status Register 3 (BICSR3)	81
• Added BIST Control and Status Register 4 (BICSR4)	81
• Changed 'RGMII_TX_DELAY_CTRL' default value in RGMII Delay Control Register (RGMIIDCTL)	82
• Changed 'RGMII_RX_DELAY_CTRL' default value in RGMII Delay Control Register (RGMIIDCTL)	82
• Added PLL Clock-out Control Register (PLLCTL).....	82
• Added DSP Feedforward Equalizer Configuration (DSP_FFE_CFG).....	83
• Changed description of '10M_SGMIII_RATE_ADAPT' in 10M SGMII Configuration (10M_SGMII_CFG)	92
• Added TDR registers 0x0190 to 0x01A4	94
• Added Programmable Gain Register (PROG_GAIN).....	99
• Changed 'PCS_RESET' description in MMD3 PCS Control Register (MMD3_PCS_CTRL).....	100
• Changed capacitor value in Figure 27 and added footnotes.....	102
• Added requirements for 2.5-V clock source capacitors in Clock In (XI) Recommendation.....	104
• Added Figure 29	104
• Added "RMS Jitter" to Table 133	104
• Added Clock Out (CLK_OUT) Phase Noise	106
• Changed capacitor placement in Figure 32 and footnote about decoupling capacitor placement.....	108
• Changed capacitor placement in Figure 33 and footnote about decoupling capacitor placement.....	109

The datasheet number will be changing.

Device Family	Change From:	Change To:
DP83867CS, DP83867IS, DP83867E	SNLS504B	SNLS504C

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/DP83867CS>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

DP83867CSRZR	DP83867CSRZT	DP83867ERZR	DP83867ERZT
DP83867ISRZR	DP83867ISRZT		

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