

PCN Number:	20200203000	PCN Date:	Feb. 18, 2020
Title:	Datasheet for MSP430FR2355, MSP430FR2353, MSP430FR2155, MSP430FR2153		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



MSP430FR2355, MSP430FR2353, MSP430FR2155, MSP430FR2153

SLASEC4D – MAY 2018 – REVISED DECEMBER 2019

Changes from March 6, 2019 to December 10, 2019

Page

• Corrected the ROM size in Figure 1-1 MSP430FR235x Functional Block Diagram and Figure 1-2 MSP430FR215x Functional Block Diagram	4
• Added a note on all VQFN pinouts to indicate that the thermal pad should be connected to VSS	11
• Corrected Figure 4-4, 32-Pin RSM (VQFN) (Top View) – MSP430FR235x	13
• Changed the note that begins "Supply voltage changes faster than 0.2 V/μs can trigger a BOR reset..." in Section 5.3, Recommended Operating Conditions	27
• Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in Section 5.3, Recommended Operating Conditions	27
• Changed the note that begins "A capacitor tolerance of ±20% or better is required..." in Section 5.3, Recommended Operating Conditions	27
• Combined former sections 5.8 and 5.10 into Section 5.9, Production Distribution of LPM Supply Currents	31
• Corrected the "SVS disabled" condition for Figure 5-1	31
• Added the note "See MSP430 32-kHz Crystal Oscillators for details on crystal section, layout, and testing" to Table 5-3, XT1 Crystal Oscillator (Low Frequency)	35
• Changed the note that begins "Requires external capacitors at both terminals..." in Table 5-3, XT1 Crystal Oscillator (Low Frequency)	35
• Added the $t_{TB, cap}$ parameter in Table 5-13, Timer_B	45
• Corrected the test conditions for the R_i parameter in Table 5-20, ADC, Power Supply and Input Range Conditions	51
• Removed ADCDIV from the equation for the ADC conversion time because ADCCLK is after division in Table 5-21, ADC, Timing Parameters	51
• Added the note that begins " $t_{Sample} = \ln(2^{n+1}) \times \tau$..." in Table 5-21, ADC, Timing Parameters	51
• Changed the unit from "nV" to "μV" for the "Input noise voltage" in the Table 5-25, SAC, OA	55
• Changed the unit from "nV/√Hz" to "nV/√Hz" for the "Input noise voltage density" in the Table 5-25, SAC, OA	55
• Removed the I_{ref} trim parameter from Table 5-27, FRAM	57
• Changed the bitfield name from RTCCLK to RTCCKSEL in the table note on Table 6-9, Clock Distribution	68
• Added Section 6.10.17, Cross-Chip Interconnection (SACx are MSP430FR235x Devices Only)	83
• Added P1SELC information in Table 6-41, Port P1, P2 Registers (Base Address: 0200h)	86
• Added P2SELC information in Table 6-41, Port P1, P2 Registers (Base Address: 0200h)	86
• Added P3SELC information in Table 6-42, Port P3, P4 Registers (Base Address: 0220h)	87
• Added P4SELC information in Table 6-42, Port P3, P4 Registers (Base Address: 0220h)	87
• Added P5SELC information in Table 6-43, Port P5, P6 Registers (Base Address: 0240h)	87
• Added P6SELC information in Table 6-43, Port P5, P6 Registers (Base Address: 0240h)	87
• Changed CRC covered end address to 0x1AF7 in table note (1) in Table 6-70, Device Descriptors	107

The datasheet number will be changing.

Device Family	Change From:	Change To:
MSP430FR2355, MSP430FR2353, MSP430FR2155, MSP430FR2153	SLASEC4C	SLASEC4D

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/MSP430FR2355>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):			
No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.			
Changes to product identification resulting from this PCN:			
None.			
Product Affected:			
MSP430FR2153TDBT	MSP430FR2155TDBTR	MSP430FR2353TDBTR	MSP430FR2355TDBTR
MSP430FR2153TDBTR	MSP430FR2155TPT	MSP430FR2353TPT	MSP430FR2355TPT
MSP430FR2153TPT	MSP430FR2155TPTR	MSP430FR2353TPTR	MSP430FR2355TPTR
MSP430FR2153TPTR	MSP430FR2155TRHAR	MSP430FR2353TRHAR	MSP430FR2355TRHAR
MSP430FR2153TRHAR	MSP430FR2155TRHAT	MSP430FR2353TRHAT	MSP430FR2355TRHAT
MSP430FR2153TRHAT	MSP430FR2155TRSMR	MSP430FR2353TRSMR	MSP430FR2355TRSMR
MSP430FR2153TRSMR	MSP430FR2155TRSMT	MSP430FR2353TRSMT	MSP430FR2355TRSMT
MSP430FR2153TRSMT	MSP430FR2353TDBT	MSP430FR2355TDBT	

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