PCN Number:	20190219001.0	PCN Date:	February 27, 2019
Title:	Datasheet for TPS659037		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

TPS659037

SLIS165G – DECEMBER 2014 – REVISED FEBRUARY 2019

Changes from Revision F (January 2018) to Revision G — **Page**

- Updated the LDOVRTC_OUT pulldown resistor recommendation to only include applicable silicon revisions. 7
- Changed ESD Ratings for charge device model on 6 pins 13
- Clarified that LDO1 and LDO2 input pins are not included in this minimum recommended operating voltage. See *Electrical Characteristics: LDO Regulators* for more information. 14
- Changed minimum recommended operating condition of OSC16MIN from 0V to -0.7V 14
- Added LDO and SMPS output capacitance footnote 15
- Changed VSYS_LO hysteresis from 95mV to 75mV 23
- Updated Caution statement to only include applicable silicon revisions. 32
- Changed discharge resistance to match electrical characteristics table 35
- Added information about shutdown timing during short circuit detection 38
- Updated POWERGOOD description to clarify multi-phase operation. 38
- Updated LDOVRTC note to only include applicable silicon revisions. 43
- Added details on identifying device version. 61
- Added typical debounce time from POWERHOLD to the enable of the first rail in the power sequence. 63
- Added VSYS_LO note for applicable silicon revisions. 74
- Updated POR requirements to only include applicable silicon revisions. 75
- SMPS and LDO output capacitance specification further explained 82
- Added design considerations for VCC1 capacitance to support loss of power 82
- Corrected 9-Vpp with 7V absolute maximum specification in the *Layout Guidelines* section 88
- Updated requirements relating to measurement of high-side and low-side FETs in the *Layout Guidelines* section 90
- Updated images and description on differential measurements across high-side and low-side FETs 90

The datasheet number will be changing.

Device Family	Change From:	Change To:
TPS659037	SLIS165F	SLIS165G

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/TPS659037

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

TPS6590376ZWSR	TPS6590376ZWST	TPS6590377ZWSR	TPS6590377ZWST
TPS6590378ZWSR	TPS6590378ZWST	TPS6590379ZWSR	TPS6590379ZWST

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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