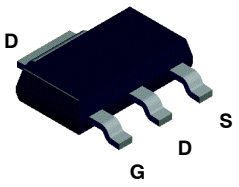
MOSFET – N-Channel, POWERTRENCH®

100 V, 6.6 A, 28 mΩ

FDT86102LZ



SOT−223
CASE 318H

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and switching loss. G−S zener has been added to enhance ESD voltage level.

Features

- Max $r_{DS(on)}$ = 28 mΩ at V_{GS} = 10 V, I_D = 6.6 A
- Max $r_{DS(on)}$ = 38 mΩ at V_{GS} = 4.5 V, I_D = 5.5 A
- HBM ESD Protection Level > 6 kV Typical (Note 4)
- Very Low Qg and Qgd Compared to Competing Trench Technologies
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb−Free, Halide Free and RoHS Compliant

Applications

- DC – DC Conversion
- Inverter
- Synchronous Rectifier

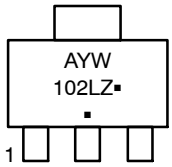
Specifications

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		100	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	−Continuous	6.6	A
		−Pulsed	40	
E_{AS}	Single Pulse Avalanche Energy (Note 3)		84	mJ
P_D	Power Dissipation	T_A = 25°C (Note 1a)	2.2	W
		T_A = 25°C (Note 1b)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

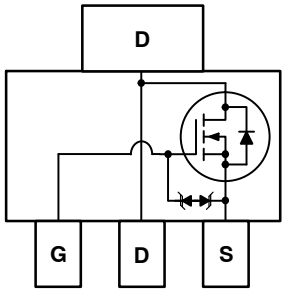
MARKING DIAGRAM



A	= Assembly Location
Y	= Year
W	= Work Week
102LZ	= Specific Device Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

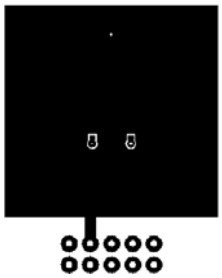
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		70		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.4	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 6.6 A		22	28	mΩ
		V_{GS} = 4.5 V, I_D = 5.5 A		27	38	
		V_{GS} = 10 V, I_D = 6.6 A, T_J = 125°C		36	46	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 6.6 A		26		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		1118	1490	pF
C_{oss}	Output Capacitance			181	245	pF
C_{rss}	Reverse Transfer Capacitance			7.5	15	pF
R_g	Gate Resistance			0.5		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 6.6 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		6.6	14	ns
t_r	Rise Time			1.9	10	ns
$t_{d(off)}$	Turn−Off Delay Time			19	31	ns
t_f	Fall Time			2.2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 6.6 A		17	25	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 50 V, I_D = 6.6 A		8.3	12	
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 6.6 A		2.6		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.2		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 6.6 A (Note 2)		0.82	1.3	V
		V_{GS} = 0 V, I_S = 1.0 A (Note 2)		0.68	1.2	
t_{rr}	Reverse Recovery Time	I_F = 6.6 A, di/dt = 100 A/μs		40	64	ns
Q_{rr}	Reverse Recovery Charge			36	58	nC

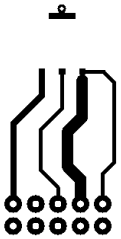
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 55°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 118°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, L = 1 mH, I_{AS} = 13 A, V_{DD} = 90 V, V_{GS} = 10 V.
4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

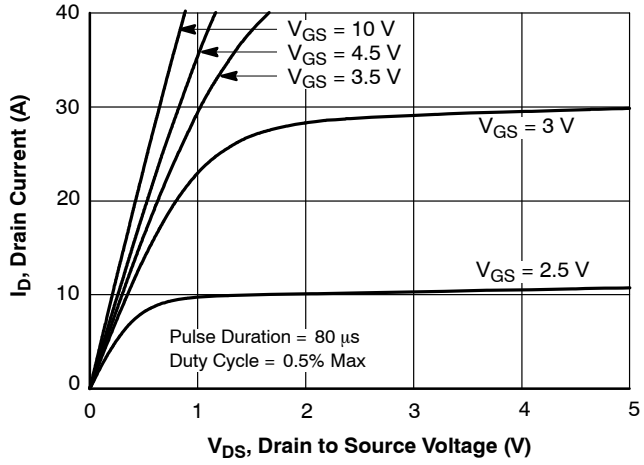


Figure 1. On Region Characteristics

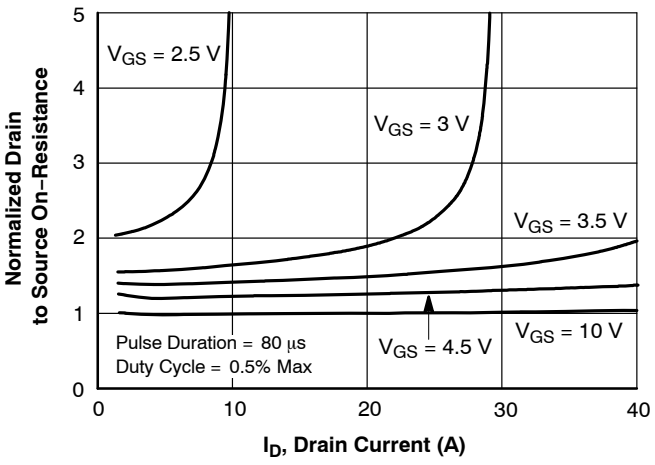


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

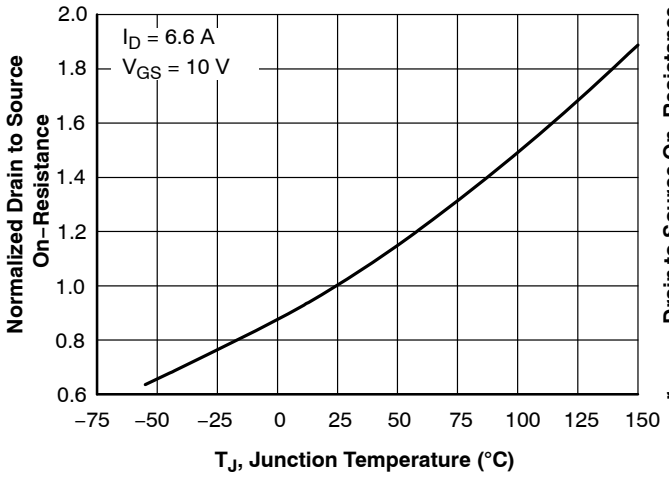


Figure 3. Normalized On Resistance vs. Junction Temperature

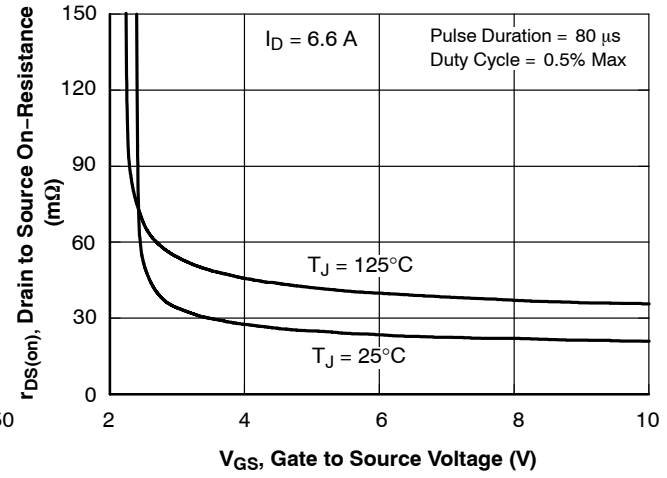


Figure 4. On−Resistance vs. Gate to Source Voltage

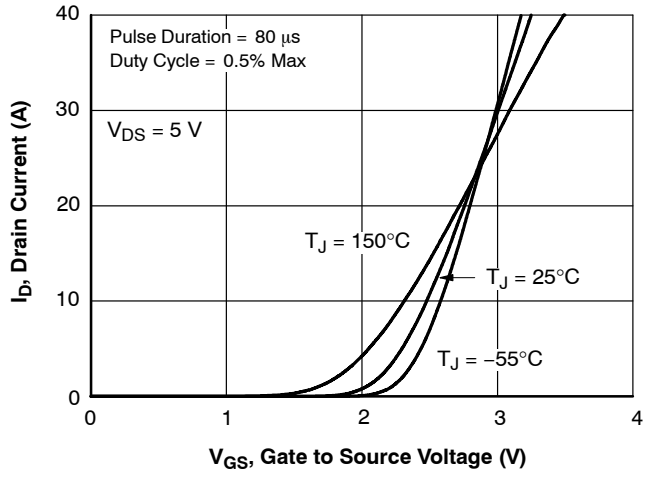


Figure 5. Transfer Characteristics

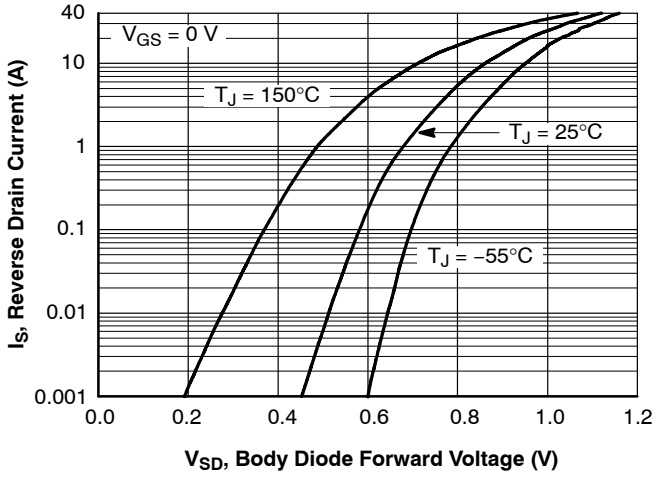


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

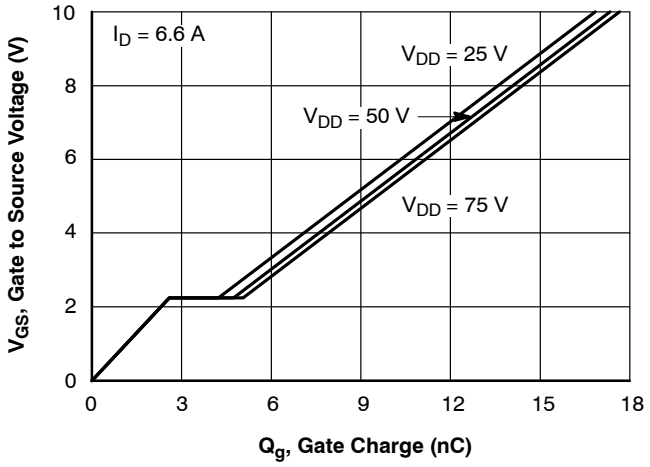


Figure 7. Gate Charge Characteristics

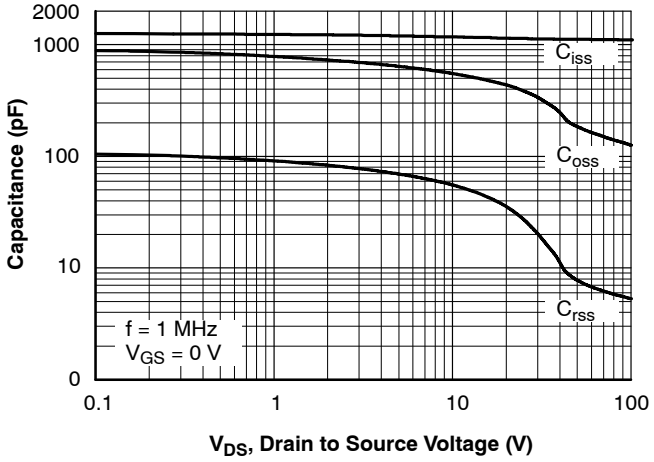


Figure 8. Capacitance vs. Drain to Source Voltage

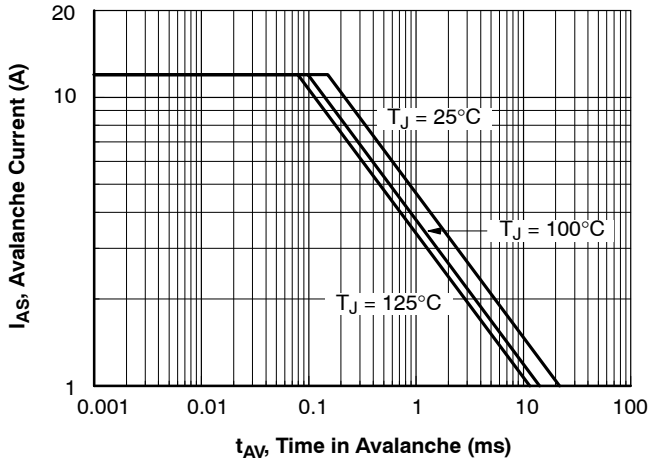


Figure 9. Unclamped Inductive Switching Capability

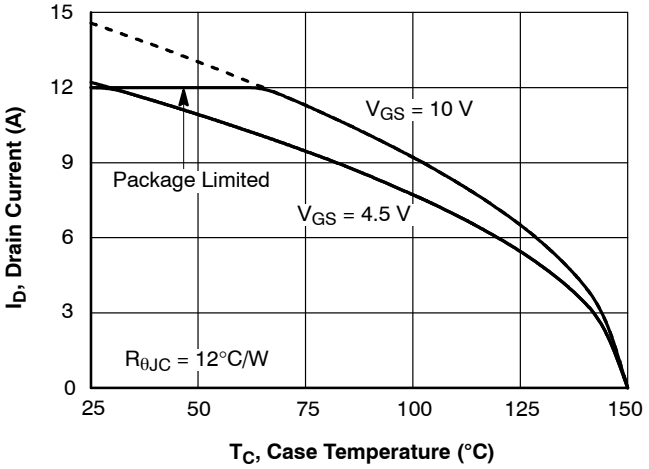


Figure 10. Maximum Continuous Drain Current vs Case Temperature

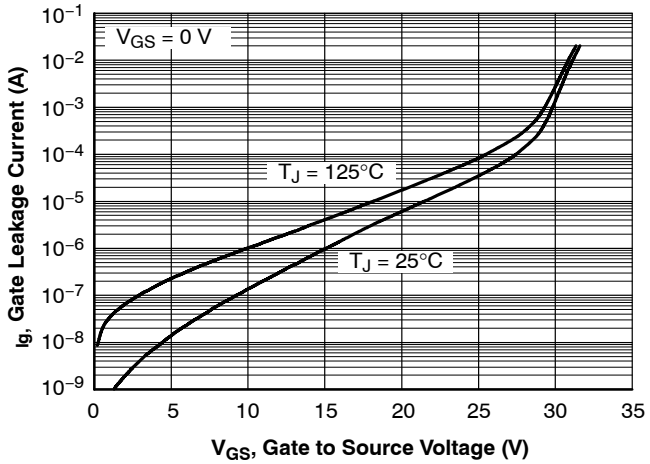


Figure 11. Gate Leakage Current vs Gate to Source Voltage

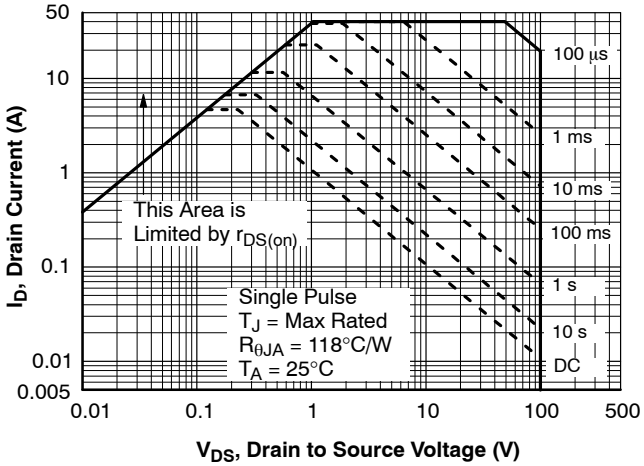


Figure 12. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

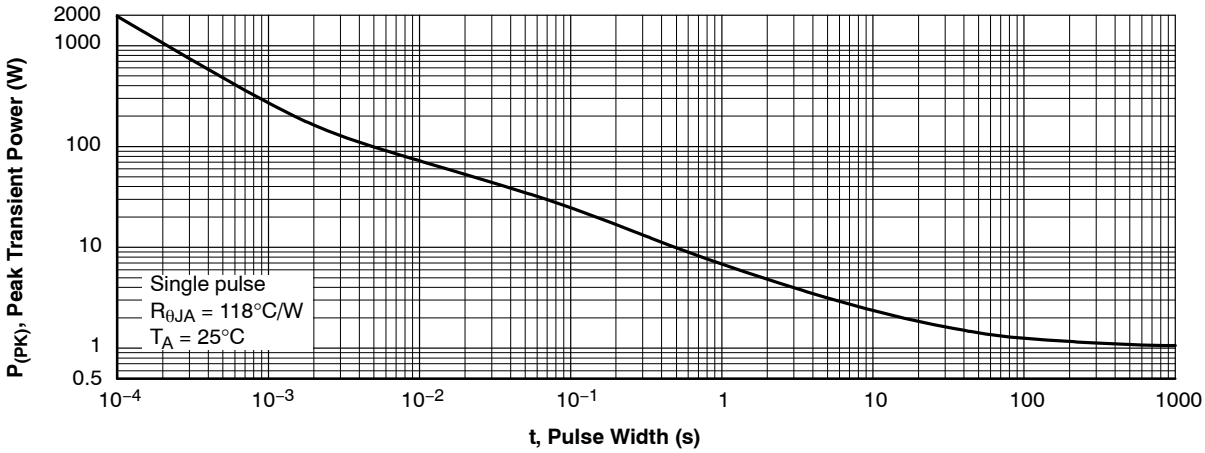


Figure 13. Single Pulse Maximum Power Dissipation

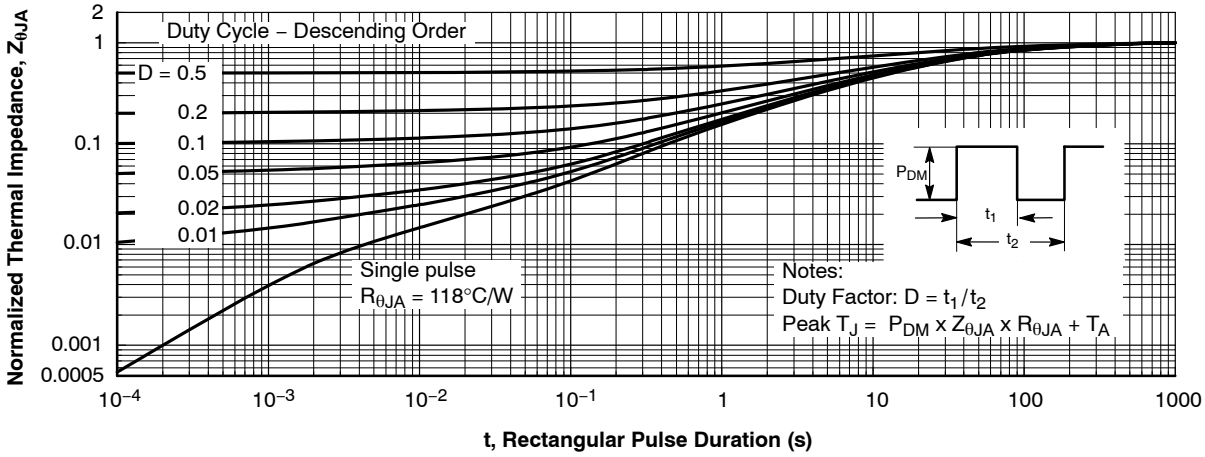


Figure 14. Junction−to−Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDT86102LZ	102LZ	SOT−223 (Pb−Free)	4000 / Tape & Reel

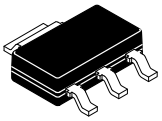
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

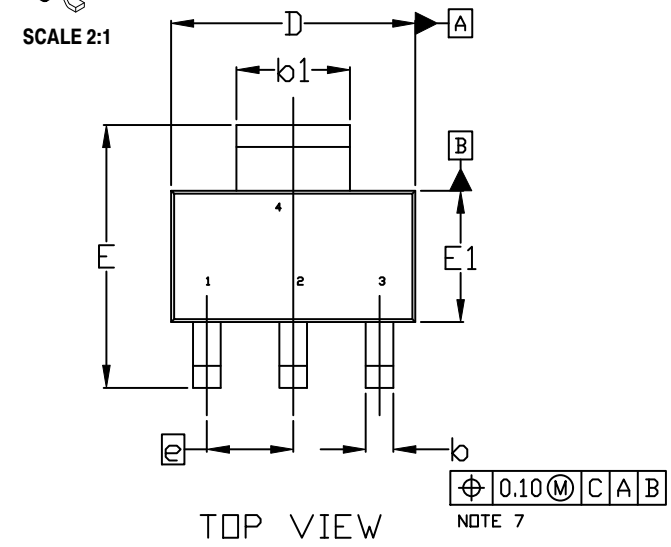
ON Semiconductor®

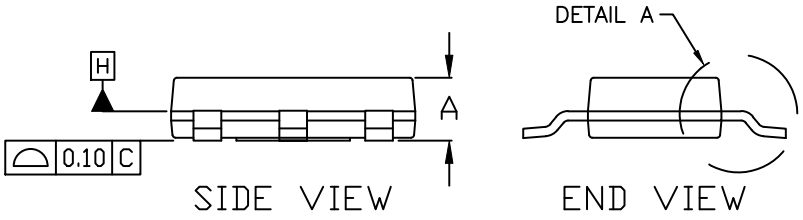
SOT−223
CASE 318H
ISSUE B

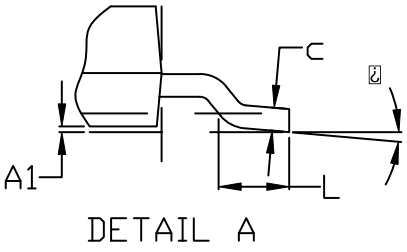
DATE 13 MAY 2020



SCALE 2:1

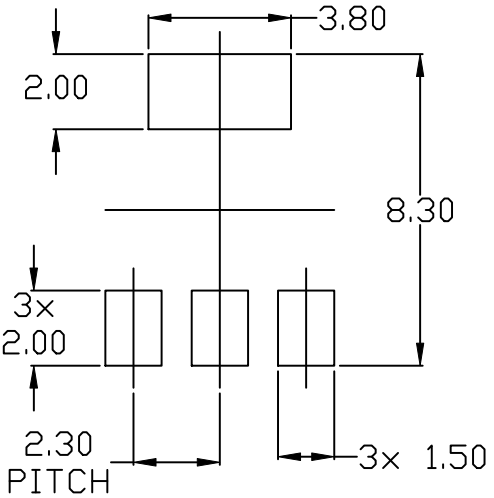






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

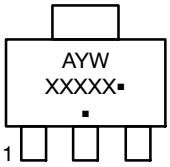
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70634A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOT−223**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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