

Tiny 500 mA, High-Speed Power MOSFET Driver

Features

- High Peak Output Current: 500 mA (typical)
- Wide Input Supply Voltage Operating Range:
 - 4.5V to 18V
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- High Capacitive Load Drive Capability:
 - 470 pF in 19 ns (typical)
 - 1000 pF in 34 ns (typical)
- Short Delay Times: 35 ns (typical)
- Matched Rise/Fall Times
- Low Supply Current:
 - With Logic '1' Input – 0.85 mA (typical)
 - With Logic '0' Input – 0.1 mA (typical)
- Latch-Up Protected: Will Withstand 500 mA Reverse Current
- Logic Input Will Withstand Negative Swing up to 5V
- Space-Saving 5-Lead SOT-23 Package

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Motor and Solenoid Drive

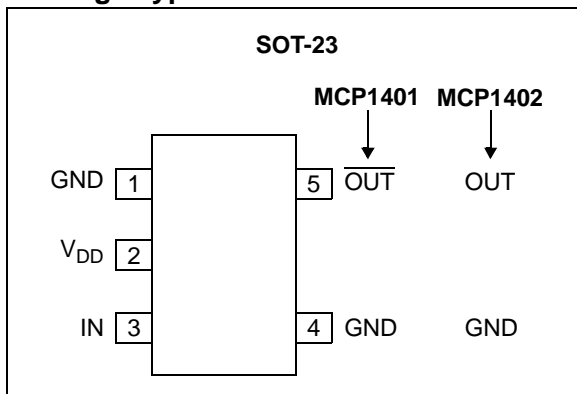
General Description

The MCP1401/02 are high-speed MOSFET drivers capable of providing 500 mA of peak current. The inverting or non-inverting single channel output is directly controlled from either TTL or CMOS (3V to 18V). These devices also feature low shoot-through current, matched rise/fall times and propagation delays which make them ideal for high switching frequency applications.

The MCP1401/02 devices operate from a single 4.5V to 18V power supply and can easily charge and discharge 470 pF gate capacitance in under 19 ns (typical). They provide low enough impedances in both the On and Off states to ensure the MOSFET's intended state will not be affected, even by large transients.

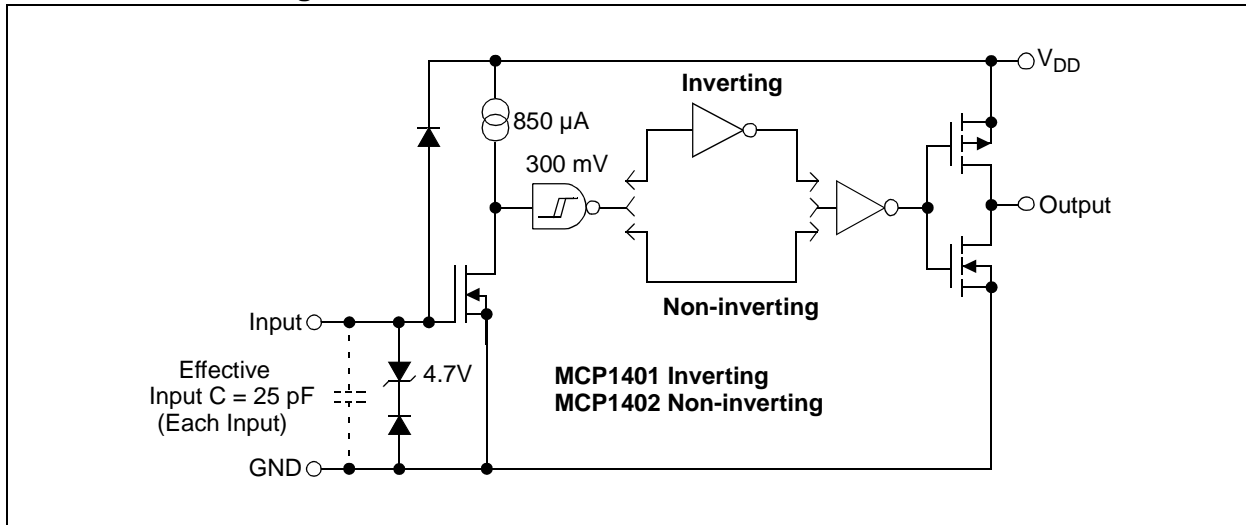
These devices are highly latch-up resistant under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the Ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current being forced back into their outputs. All terminals are fully protected against Electrostatic Discharge (ESD) up to 1 kV (HBM) and 300V (MM).

Package Types



MCP1401/02

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

| | |
|--|-----------------------------------|
| Supply Voltage | +20V |
| Input Voltage | ($V_{DD} + 0.3V$) to (GND – 5V) |
| Input Current ($V_{IN} > V_{DD}$) | 50 mA |
| Package Power Dissipation ($T_A = 50^\circ C$) | |
| SOT-23-5 | 0.39W |

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (Note 2)

| Electrical Specifications: Unless otherwise indicated, $T_A = +25^\circ C$, with $4.5V \leq V_{DD} \leq 18V$. | | | | | | |
|---|-----------|------------------|-------|----------------|----------|---|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
| Input | | | | | | |
| Logic '1', High Input Voltage | V_{IH} | 2.4 | 1.5 | — | V | |
| Logic '0', Low Input Voltage | V_{IL} | — | 1.3 | 0.8 | V | |
| Input Current | I_{IN} | -1 | — | 1 | μA | $0V \leq V_{IN} \leq V_{DD}$ |
| Input Voltage | V_{IN} | -5 | — | $V_{DD} + 0.3$ | V | |
| Output | | | | | | |
| High Output Voltage | V_{OH} | $V_{DD} - 0.025$ | — | — | V | DC Test |
| Low Output Voltage | V_{OL} | — | — | 0.025 | V | DC Test |
| Output Resistance, High | R_{OH} | — | 12 | 18 | Ω | $I_{OUT} = 10\text{ mA}$, $V_{DD} = 18V$ |
| Output Resistance, Low | R_{OL} | — | 10 | 16 | Ω | $I_{OUT} = 10\text{ mA}$, $V_{DD} = 18V$ |
| Peak Output Current | I_{PK} | — | 0.5 | — | A | $V_{DD} = 18V$ (Note 2) |
| Latch-Up Protection Withstand Reverse Current | I_{REV} | — | > 0.5 | — | A | Duty cycle $\leq 2\%$, $t \leq 300\ \mu s$ |
| Switching Time (Note 1) | | | | | | |
| Rise Time | t_R | — | 19 | 25 | ns | Figure 4-1, Figure 4-2 $C_L = 470\text{ pF}$ |
| Fall Time | t_F | — | 15 | 20 | ns | Figure 4-1, Figure 4-2 $C_L = 470\text{ pF}$ |
| Delay Time | t_{D1} | — | 35 | 40 | ns | Figure 4-1, Figure 4-2 |
| Delay Time | t_{D2} | — | 35 | 40 | ns | Figure 4-1, Figure 4-2 |
| Power Supply | | | | | | |
| Supply Voltage | V_{DD} | 4.5 | — | 18.0 | V | |
| Power Supply Current | I_S | — | 0.85 | 1.1 | mA | $V_{IN} = 3V$ |
| | I_S | — | 0.10 | 0.20 | mA | $V_{IN} = 0V$ |

Note 1: Switching times ensured by design.

2: Tested during characterization, not production tested.

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DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

| Electrical Specifications: Unless otherwise indicated, operating temperature range with $4.5V \leq V_{DD} \leq 18V$. | | | | | | |
|---|----------|------------------|------|----------------|----------|--|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
| Input | | | | | | |
| Logic '1', High Input Voltage | V_{IH} | 2.4 | — | — | V | |
| Logic '0', Low Input Voltage | V_{IL} | — | — | 0.8 | V | |
| Input Current | I_{IN} | -10 | — | +10 | μA | $0V \leq V_{IN} \leq V_{DD}$ |
| Input Voltage | V_{IN} | -5 | — | $V_{DD} + 0.3$ | V | |
| Output | | | | | | |
| High Output Voltage | V_{OH} | $V_{DD} - 0.025$ | — | — | V | DC TEST |
| Low Output Voltage | V_{OL} | — | — | 0.025 | V | DC TEST |
| Output Resistance, High | R_{OH} | — | 16 | 18 | Ω | $I_{OUT} = 10 \text{ mA}$, $V_{DD} = 18V$ |
| Output Resistance, Low | R_{OL} | — | 16 | 19 | Ω | $I_{OUT} = 10 \text{ mA}$, $V_{DD} = 18V$ |
| Switching Time (Note 1) | | | | | | |
| Rise Time | t_R | — | 20 | 30 | ns | Figure 4-1, Figure 4-2 $C_L = 470 \text{ pF}$ |
| Fall Time | t_F | — | 18 | 28 | ns | Figure 4-1, Figure 4-2 $C_L = 470 \text{ pF}$ |
| Delay Time | t_{D1} | — | 40 | 51 | ns | Figure 4-1, Figure 4-2 |
| Delay Time | t_{D2} | — | 40 | 51 | ns | Figure 4-1, Figure 4-2 |
| Power Supply | | | | | | |
| Supply Voltage | V_{DD} | 4.5 | — | 18.0 | V | |
| Power Supply Current | I_S | — | 0.90 | 1.10 | mA | $V_{IN} = 3V$ |
| | | — | 0.11 | 0.20 | mA | $V_{IN} = 0V$ |

Note 1: Switching times ensured by design.

Note 2: Tested during characterization, not production tested.

TEMPERATURE CHARACTERISTICS

| Electrical Specifications: Unless otherwise noted, all parameters apply with $4.5V \leq V_{DD} \leq 18V$. | | | | | | |
|--|---------------|------|-------|------|---------------|------------|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
| Temperature Ranges | | | | | | |
| Specified Temperature Range | T_A | -40 | — | +125 | $^{\circ}C$ | |
| Maximum Junction Temperature | T_J | — | — | +150 | $^{\circ}C$ | |
| Storage Temperature Range | T_A | -65 | — | +150 | $^{\circ}C$ | |
| Package Thermal Resistances | | | | | | |
| Thermal Resistance, 5L-SOT-23 | θ_{JA} | — | 220.7 | — | $^{\circ}C/W$ | |

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

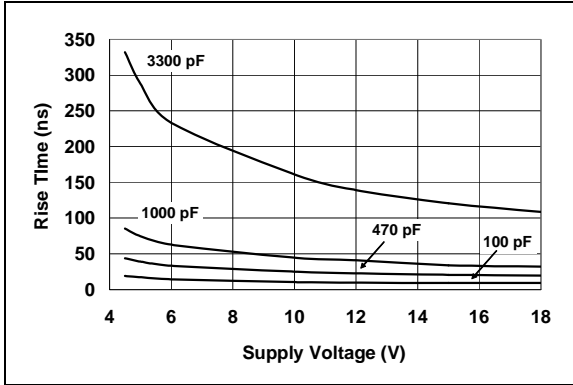


FIGURE 2-1: Rise Time vs. Supply Voltage.

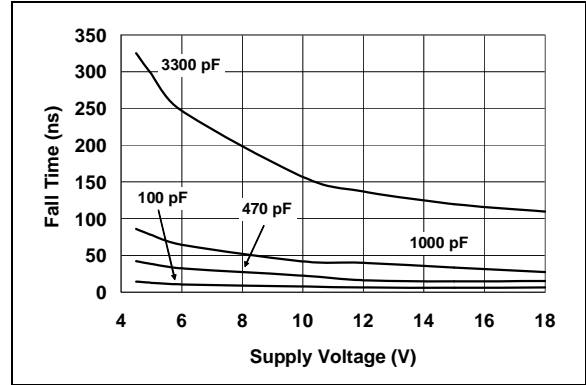


FIGURE 2-4: Fall Time vs. Supply Voltage.

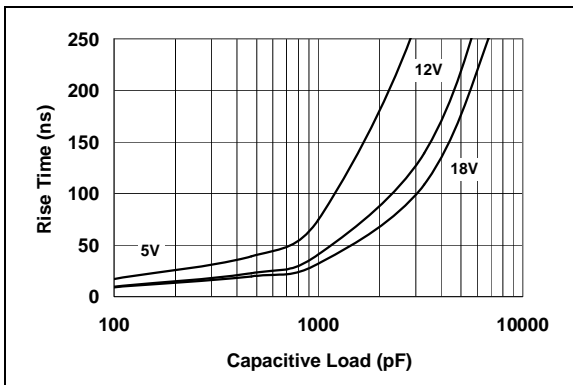


FIGURE 2-2: Rise Time vs. Capacitive Load.

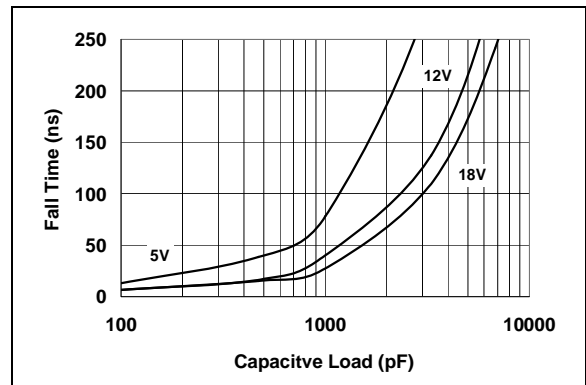


FIGURE 2-5: Fall Time vs. Capacitive Load.

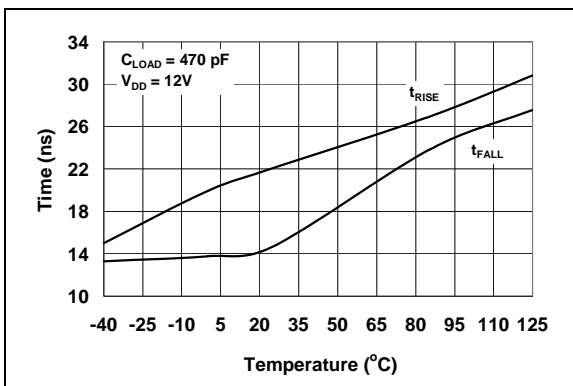


FIGURE 2-3: Rise and Fall Times vs. Temperature.

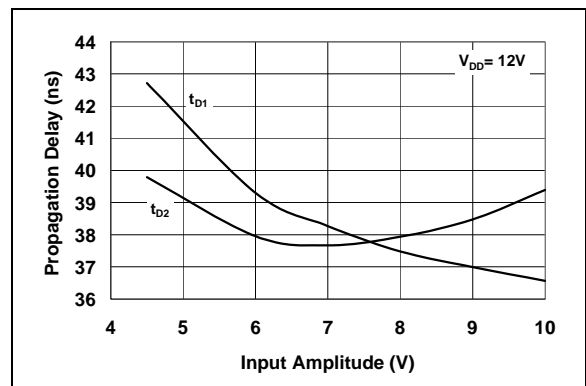


FIGURE 2-6: Propagation Delay vs. Input Amplitude.

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

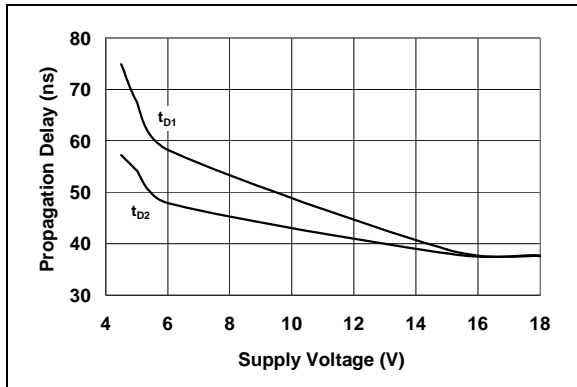


FIGURE 2-7: Propagation Delay Time vs. Supply Voltage.

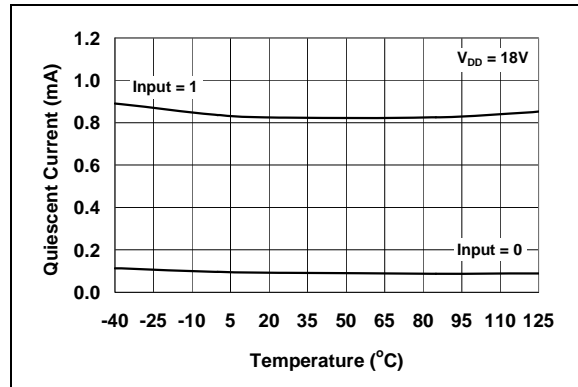


FIGURE 2-10: Quiescent Current vs. Temperature.

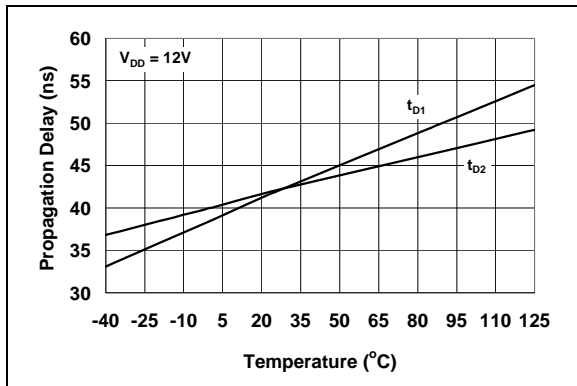


FIGURE 2-8: Propagation Delay Time vs. Temperature.

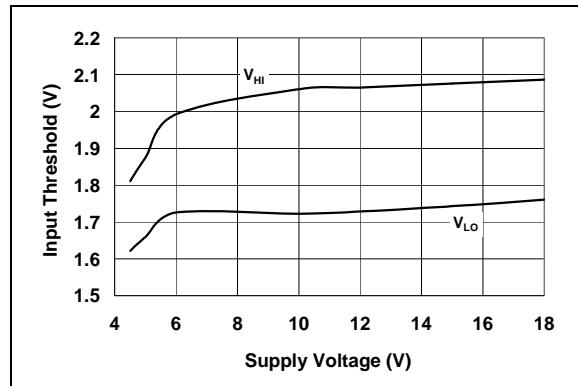


FIGURE 2-11: Input Threshold vs. Supply Voltage.

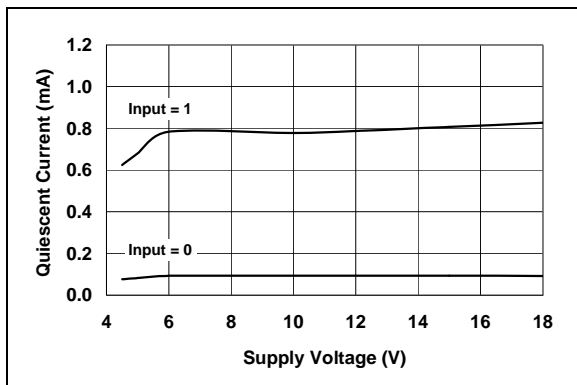


FIGURE 2-9: Quiescent Current vs. Supply Voltage.

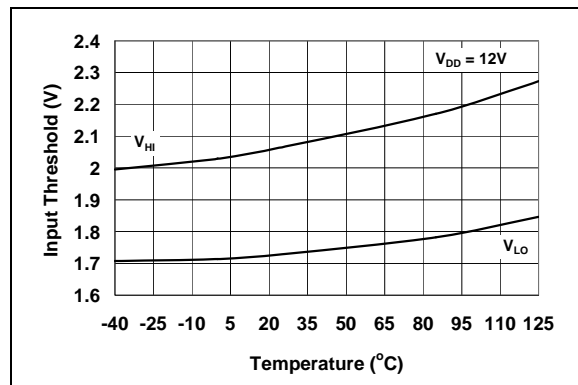


FIGURE 2-12: Input Threshold vs. Temperature.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

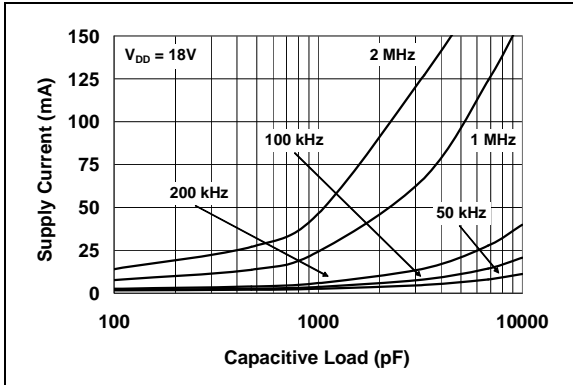


FIGURE 2-13: Supply Current vs. Capacitive Load.

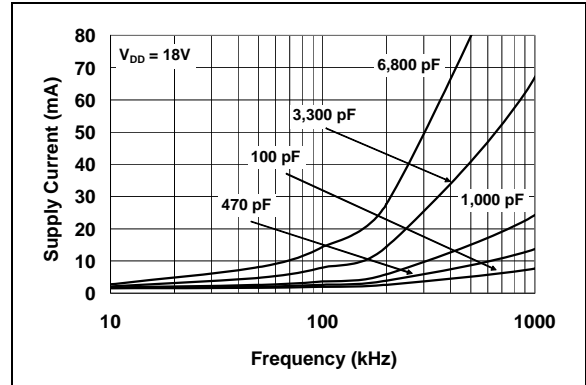


FIGURE 2-16: Supply Current vs. Frequency.

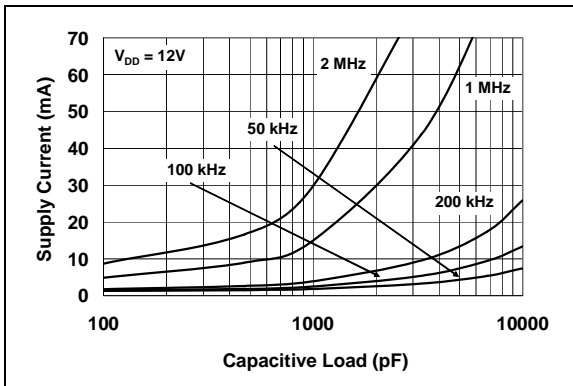


FIGURE 2-14: Supply Current vs. Capacitive Load.

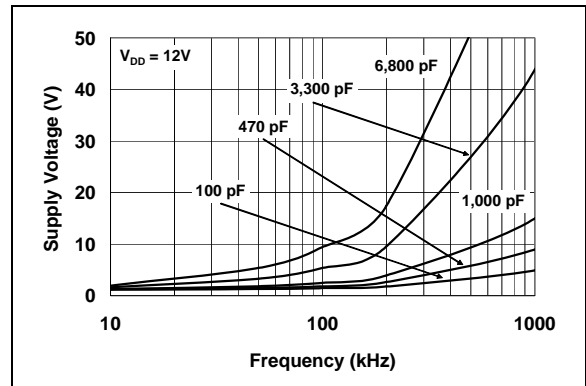


FIGURE 2-17: Supply Current vs. Frequency.

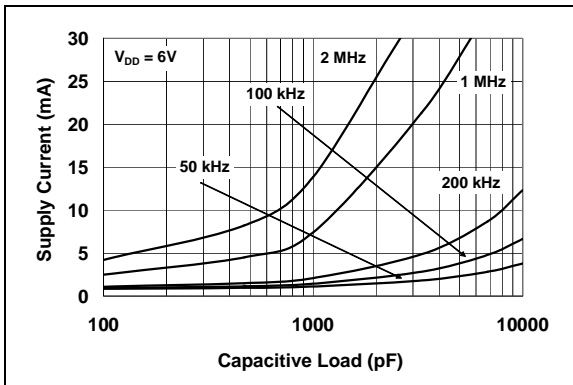


FIGURE 2-15: Supply Current vs. Capacitive Load.

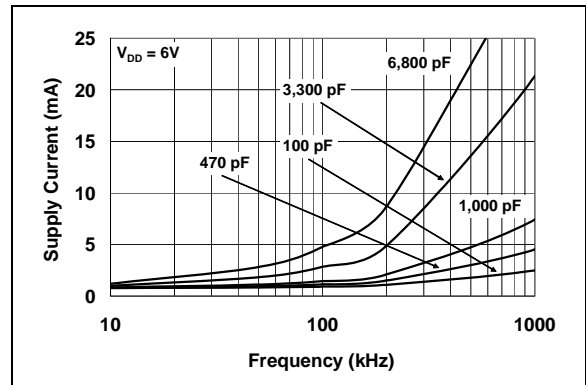


FIGURE 2-18: Supply Current vs. Frequency.

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

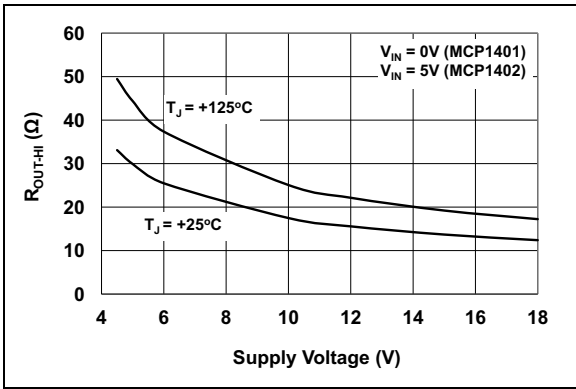


FIGURE 2-19: Output Resistance (Output High) vs. Supply Voltage.

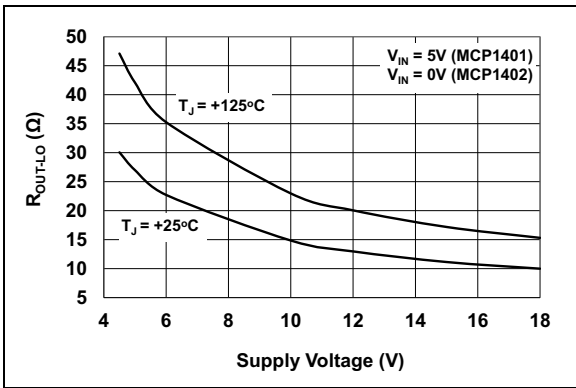


FIGURE 2-20: Output Resistance (Output Low) vs. Supply Voltage.

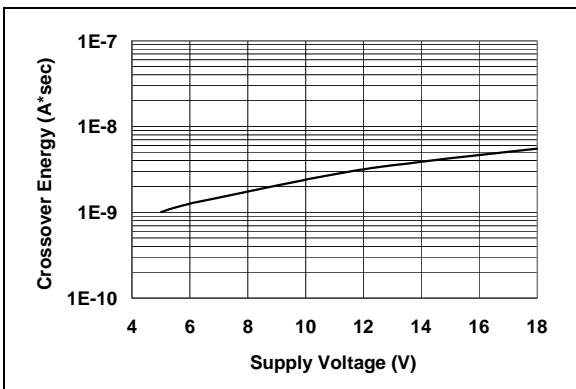


FIGURE 2-21: Crossover Energy vs. Supply Voltage.

3.0 PIN DESCRIPTIONS

The description of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE⁽¹⁾

| Pin No. | MCP1401 | MCP1402 | Description |
|---------|-------------------------|-----------------|---------------|
| 1 | GND | GND | Ground |
| 2 | V _{DD} | V _{DD} | Supply Input |
| 3 | IN | IN | Control Input |
| 4 | GND | GND | Ground |
| 5 | $\overline{\text{OUT}}$ | OUT | Output |

Note 1: Duplicate pins must be connected for proper operation.

3.1 Supply Input (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are to be provided to the load.

3.2 Control Input (IN)

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input also has hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity.

3.3 Ground (GND)

Ground is the Device Return pin. The Ground pin should have a low-impedance connection to the bias supply source return. High peak currents will flow out the Ground pin when the capacitive load is being discharged.

3.4 Output (OUT, $\overline{\text{OUT}}$)

The output is a CMOS push-pull output that is capable of sourcing and sinking 0.5A of peak current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. This output also has a reverse current latch-up rating of 0.5A.

MCP1401/02

4.0 APPLICATION INFORMATION

4.1 General Information

MOSFET drivers are high-speed, high-current devices which are intended to source/sink high peak currents to charge/discharge the gate capacitance of external MOSFETs or IGBTs. In high-frequency switching power supplies, the PWM controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver like the MCP1401/02 family can be used to provide additional source/sink current capability.

4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully-off state to a fully-on state is characterized by the driver's rise time (t_R), fall time (t_F), and propagation delays (t_{D1} and t_{D2}). The MCP1401/02 family of drivers can typically charge and discharge a 470 pF load capacitance in 19 ns, along with a typical matched propagation delay of 35 ns. Figures 4-1 and 4-2 show the test circuit and timing waveform used to verify the MCP1401/02 timing.

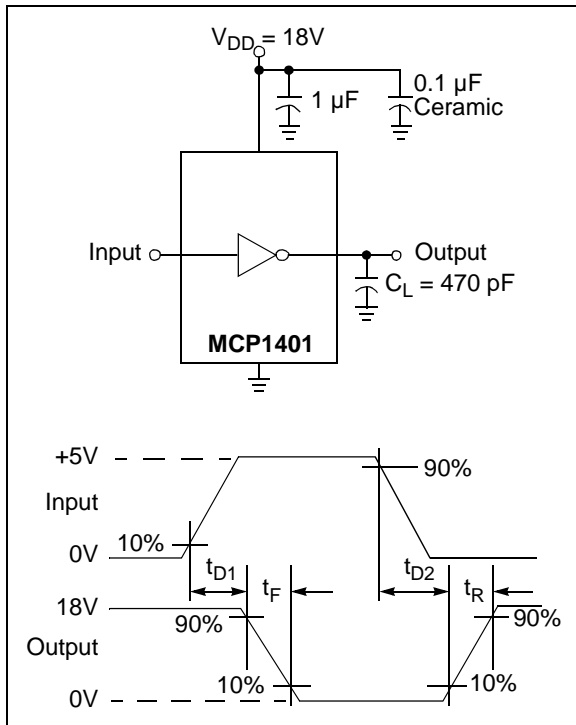


FIGURE 4-1: Inverting Driver Timing Waveform.

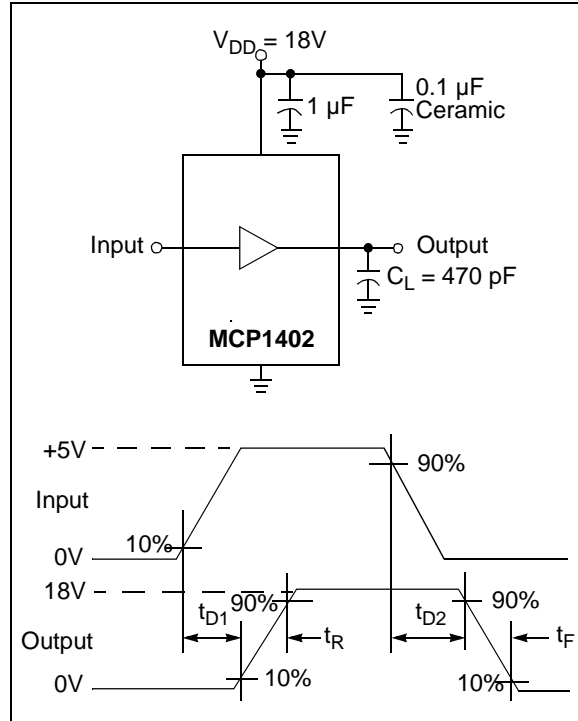


FIGURE 4-2: Non-Inverting Driver Timing Waveform.

4.3 Decoupling Capacitors

Careful layout and decoupling capacitors are highly recommended when using MOSFET drivers. Large currents are required to charge and discharge capacitive loads quickly. For example, approximately 550 mA are needed to charge a 470 pF load with 18V in 15 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, it is recommended to place a ceramic and low ESR film capacitor in parallel between the driver V_{DD} and GND. A 1.0 μF low ESR film capacitor and a 0.1 μF ceramic capacitor placed between pins 2 and 1 should be used. These capacitors should be placed close to the driver to minimize circuit board parasitics and provide a local source for the required current.

4.4 PCB Layout Considerations

Proper Printed Circuit Board (PCB) layout is important in a high-current, fast switching circuit to provide proper device operation and robustness of design. PCB trace loop area and inductance should be minimized by the use of ground planes or trace under MOSFET gate drive signals, separate analog and power grounds, and local driver decoupling.

Placing a ground plane beneath the MCP1401/02 will help as a radiated noise shield and it will provide some heat sinking for power dissipated within the device.

4.5 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements.

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

| | | |
|----------|---|-----------------------------|
| P_T | = | Total power dissipation |
| P_L | = | Load power dissipation |
| P_Q | = | Quiescent power dissipation |
| P_{CC} | = | Operating power dissipation |

4.5.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of frequency, total capacitive load, and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is shown in [Equation 4-2](#).

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

| | | |
|----------|---|------------------------------|
| f | = | Switching frequency |
| C_T | = | Total load capacitance |
| V_{DD} | = | MOSFET driver supply voltage |

4.5.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends upon the state of the Input pin. The MCP1401/02 devices have a quiescent current draw of 0.85 mA (typical) when the input is high and of 0.1 mA (typical) when the input is low. The quiescent power dissipation is shown in [Equation 4-3](#).

EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

| | | |
|----------|---|-------------------------------------|
| I_{QH} | = | Quiescent current in the high state |
| D | = | Duty cycle |
| I_{QL} | = | Quiescent current in the low state |
| V_{DD} | = | MOSFET driver supply voltage |

4.5.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions because, for a very short period of time, both MOSFETs in the output stage are on simultaneously. This cross-conduction current leads to a power dissipation described in [Equation 4-4](#).

EQUATION 4-4:

$$P_{CC} = CC \times f \times V_{DD}$$

Where:

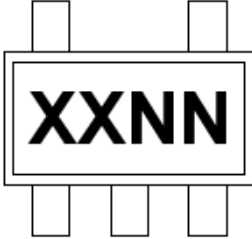
| | | |
|----------|---|-------------------------------------|
| CC | = | Cross-conduction constant (A * sec) |
| f | = | Switching frequency |
| V_{DD} | = | MOSFET driver supply voltage |

MCP1401/02

5.0 PACKAGING INFORMATION

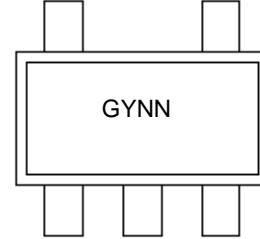
5.1 Package Marking Information

5-Lead SOT-23



| Standard Markings for SOT-23 | |
|------------------------------|------|
| Part Number | Code |
| MCP1401T-E/OT | GYNN |
| MCP1402T-E/OT | GZNN |

Example

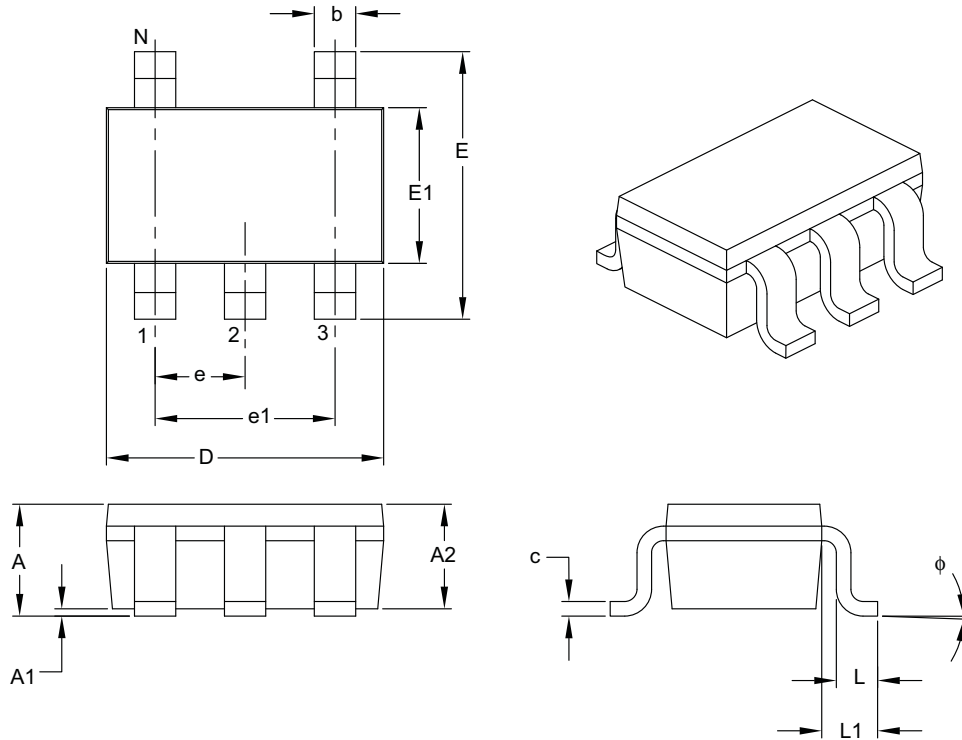


| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 5 | | |
| Lead Pitch | e | 0.95 BSC | | |
| Outside Lead Pitch | e1 | 1.90 BSC | | |
| Overall Height | A | 0.90 | – | 1.45 |
| Molded Package Thickness | A2 | 0.89 | – | 1.30 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | 2.20 | – | 3.20 |
| Molded Package Width | E1 | 1.30 | – | 1.80 |
| Overall Length | D | 2.70 | – | 3.10 |
| Foot Length | L | 0.10 | – | 0.60 |
| Footprint | L1 | 0.35 | – | 0.80 |
| Foot Angle | ϕ | 0° | – | 30° |
| Lead Thickness | c | 0.08 | – | 0.26 |
| Lead Width | b | 0.20 | – | 0.51 |

Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

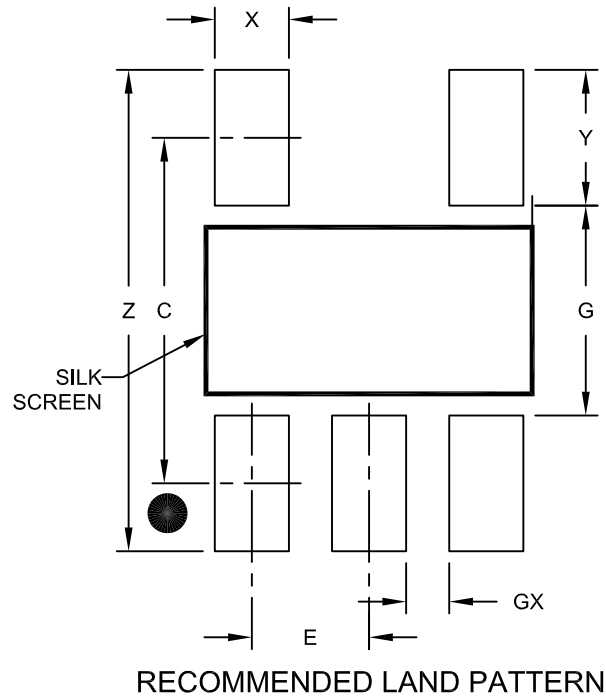
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

MCP1401/02

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.95 BSC | | |
| Contact Pad Spacing | C | | 2.80 | |
| Contact Pad Width (X5) | X | | | 0.60 |
| Contact Pad Length (X5) | Y | | | 1.10 |
| Distance Between Pads | G | 1.70 | | |
| Distance Between Pads | GX | 0.35 | | |
| Overall Width | Z | | | 3.90 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

APPENDIX A: REVISION HISTORY

Revision D (June 2014)

The following is the list of modifications:

1. Updated [Figure 2-19](#) and [Figure 2-20](#).

Revision C (September 2013)

The following is the list of modifications:

1. Updated values for Electrostatic Discharge (ESD) protection in the **Section “General Description”**.
2. Updated package drawings in [Section 5.0 “Packaging Information”](#).
3. Updated ROH and ROL numbers in the **“DC Characteristics (Over Operating Temperature Range)”** table.

Revision B (December 2007)

The following is the list of modifications:

1. Updated the low supply current values.
2. Updated [Section 5.1 “Package Marking Information”](#).

Revision A (June 2007)

- Original Release of this Document.

MCP1401/02

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | X | X | XX |
|---------------------------|--|-------------------|---------|
| Device | Tape & Reel Range | Temperature Range | Package |
| Device: | MCP1401: 500 mA MOSFET Driver, Inverting MCP1402: 500 mA MOSFET Driver, Non-Inverting | | |
| Tape and Reel: | T = Tape and Reel | | |
| Temperature Range: | E = -40°C to +125°C | | |
| Package: * | OT = Plastic Thin Small Outline Transistor (OT), 5-Lead * All package offerings are Pb Free (Lead Free) | | |

Examples:

- a) MCP1401T-E/OT: 500 mA Inverting MOSFET Driver, 5LD SOT-23 package.
- a) MCP1402T-E/OT: 500 mA Non-Inverting MOSFET Driver, 5LD SOT-23 package.

MCP1401/02

NOTES:

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