On-Resistance Load Switch 5.5 V, 3.9 mΩ, 10 A

NLPS22990, NLPS22990N

The NLPS22990 and NLPS22990N devices are 3.9 mΩ, single−channel load switches with controlled and adjustable turn ons and integrated PG indicators.

Each device is an N−channel MOSFET operating over an input voltage range of 0.6 V to 5.5 V. The switch supports a maximum continuous current of 10 A. 3.9 mΩ switch on resistance minimizes both the voltage drop across the load switch and the power loss from the load switch.

Controlled rise time of the device switch reduces inrush currents caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. Adjustable slew rate through CT provides the design flexibility to trade off inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

The NLPS22990 has a 200−Ω On−chip resistor for quick discharge of the output when switch is disabled. This avoids unknown state caused by floating supply to the downstream load.

Features

- Integrated Single Channel Load Switch
- V_{BIAS} Voltage Range: 2.5 V to 5.5 V
- V_{IN} Voltage Range: 0.6 V to VBIAS
- On−Resistance
  - R_{ON} = 3.9 mΩ (typical) at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 3.9 mΩ (typical) at V_{IN} = 3.3 V (V_{BIAS} = 3.3 V)
- 10−A Maximum Continuous Switch Current
- Quiescent Current
  - $I_{Q,VBIAS}$ = 85 μA at V_{BIAS} = 5 V
- Shutdown Current
  - $I_{SD,VBIAS}$ = 0.3 μA at V_{BIAS} = 5 V
  - $I_{SD,VIN}$ = 1.3 μA at V_{BIAS} = 5 V, V_{IN} = 5 V
- Controlled and Adjustable Slew Rate through CT
- Power Good (PG) Indicator
- Quick Output Discharge (QOD) (NLPS22990 Only)
- 3−mm x 2−mm WQFN 10−pin Package with Thermal Pad
- ESD Performance Tested per JESD 22
  - 2 kV HBM and 1 kV CDM

Applications

- Notebooks, Chromebooks and Tablets
- Desktop PC and Industrial PC
- Solid State Drives (SSDs)
- Servers
- Telecom Systems

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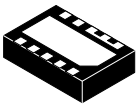
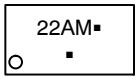


WDFN10
MN SUFFIX
CASE 511DX

MARKING DIAGRAM



22A = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NLPS22990MN1TAG	WDFN10 (Pb−Free)	3000 / Tape & Reel
NLPS22990NMN1TAG (In development)		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

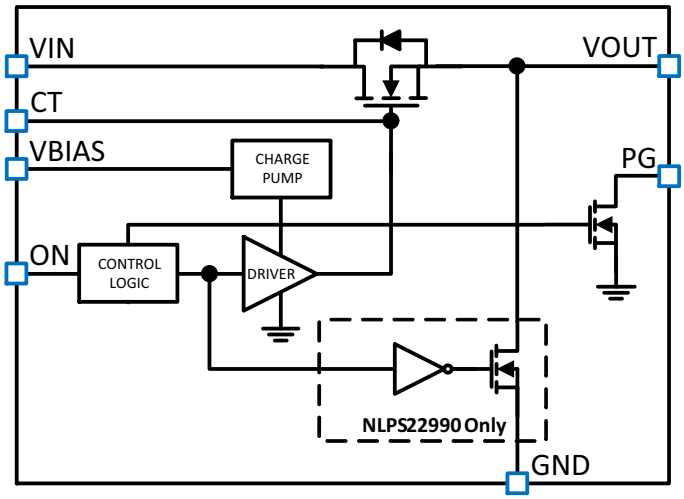


Figure 1. Block Diagram

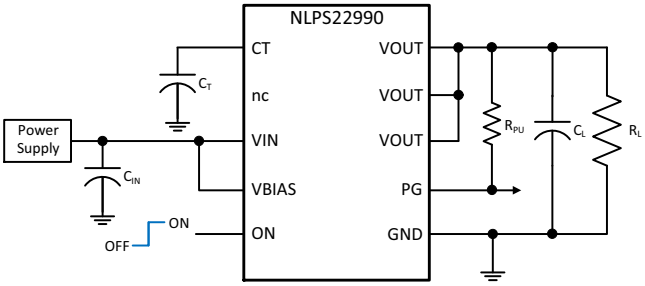


Figure 2. Typical Application

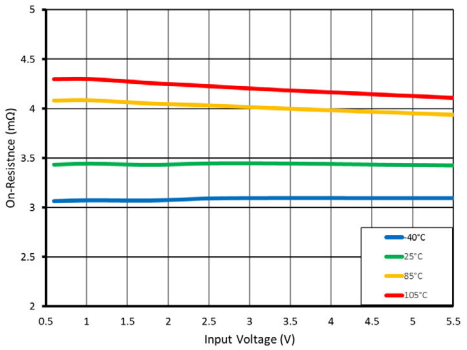


Figure 3. On Resistance vs. Input Voltage

DEVICE COMPARISON

Device	R_{ON} at V_{BIAS} = 5 V	I_{MAX}	ENABLE	QOD
NLPS22990	3.9 mΩ	10 A	Active High	Yes
NLPS22990N	3.9 mΩ	10 A	Active High	No

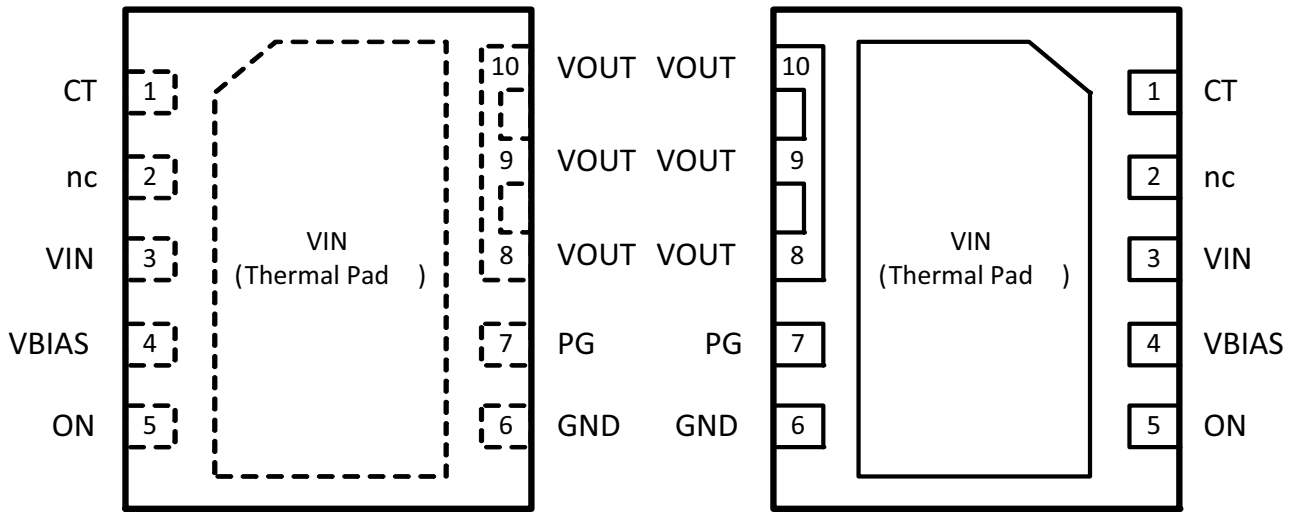


Figure 4. WDFN10 Pin Assignment

Table 1. PIN DESCRIPTIONS

Pin Name	Pin	Pin Type	Description
CT	1	O	V_{OUT} slew rate control.
nc	2	–	No connect.
V_{IN}	3	I	Switch input. Bypass this input with a ceramic capacitor to GND.
V_{BIAS}	4	P	Bias voltage. Power supply to the device.
ON	5	I	Active high switch control input. Do not leave floating.
GND	6	GND	Device ground.
PG	7	O	Power good. Active high open−drain output. Tie to GND if not used.
V_{OUT}	8	O	Switch output.
	9		
	10		
V_{IN}	Thermal Pad	I	Switch input. VIN and thermal pad (exposed center pad) to alleviate thermal stress. See the layout section for layout guidelines.

Table 2. MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{BIAS}	Bias Voltage	−0.3 to +6	V
V_{IN}	Input Voltage	−0.3 to +6	V
V_{OUT}	Output Voltage	−0.3 to +6	V
V_{ON}	ON Voltage	−0.3 to +6	V
V_{PG}	PG Voltage	−0.3 to +6	V
V_{CT}	CT Voltage	−0.3 to +15	V
I_{MAX}	Continuous Switch Current at T_J = 125°C	10	A
I_{PLS}	Pulsed Switch Current, Pulse < 300 μs 2% Duty Cycle	12	A
V_{IN}	Digital Control Pin Voltage on EN, SEL	−0.5 to V_{CC}+0.5	V
T_s	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	300	°C
T_J	Junction Temperature	125	°C
MSL	Moisture Sensitivity (Note 1)	Level 1	
ESD	ESD Protection (Note 2)		V
	Human Body Model	±2000	
	Charged Device Model	±1000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Charged Device Model (CDM) ±1000 V per JEDEC standard: JESD22−C101.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{BIAS}	Bias Voltage	2.5	5.5	V
V_{IN}	Input Voltage	0.6	V_{BIAS}	V
V_{OUT}	Output Voltage		V_{IN}	V
V_{ON}	ON Voltage	0	5.5	V
V_{PG}	PG Voltage	0	5.5	V
C_{IN}	Input Capacitor (Note 3)	1		μF
T_A	Operating Temperature Range	−40	+105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. See Application Information section.

Table 4. THERMAL INFORMATION

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction to Ambient Thermal Resistance	51.4	°C/W
$R_{\theta JC(top)}$	Junction to Case (top) Thermal Resistance	65	°C/W
$R_{\theta JB}$	Junction to Board Thermal Resistance	17.4	°C/W
ψ_{JT}	Junction to Top Characterization Parameter	2.1	°C/W
ψ_{JB}	Junction to Bottom Characterization Parameter	17	°C/W
$R_{\theta JC(bot)}$	Junction to Case (bottom) Thermal Resistance	3.7	°C/W

4. See Application Information section.

Table 5. DC ELECTRICAL CHARACTERISTICS (Typical values are at T_A = +25°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	V_{BIAS} (V)	–40°C to 85°C			–40°C to 105°C		Unit
				Min	Typ	Max	Min	Max	
ON PIN									
V_{IH}	Input Voltage High		5, 3.3	1.0	–	5.5	1.0	5.5	V
V_{IL}	Input Voltage Low		5, 3.3	0	–	0.5	0	0.5	V
V_{HYS}	Hysteresis Voltage		5	–	99	–	–	–	mV
			3.3	–	128	–	–	–	
$I_{ON,LKG}$	Input Leakage Current		5, 3.3	–	–	0.1	–	0.1	μA
PG PIN									
V_{OL}	Output Voltage Low	V_{ON} = 0 V, I_{PG} = 1 mA	5, 3.3	–	–	0.2	–	0.2	V
$I_{PG,LKG}$	Leakage Current into Pin	V_{PG} = 5 V	5, 3.3	–	–	0.5	–	0.5	μA
POWER SUPPLY AND OTHER CURRENTS									
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current	I_{OUT} = 0 A,							μA
		V_{IN} = V_{ON} = 5 V	5	–	85	100	–	100	
		V_{IN} = V_{ON} = 3.3 V	3.3	–	63	80	–	80	
$I_{SD,VBIAS}$	V_{BIAS} Shutdown Current	V_{ON} = 0 V, V_{OUT} = 0 V	5	–	0.3	7	–	7	μA
			3.3	–	0.3	6	–	7	
$I_{SD,VIN}$	V_{IN} Shutdown Current	V_{ON} = 0 V, V_{OUT} = 0 V,	5						μA
		V_{IN} = 5 V		–	1.3	4	–	10	
		V_{IN} = 3.3 V		–	0.8	3	–	7	
		V_{IN} = 2.5 V		–	0.6	2	–	5	
		V_{IN} = 1.8 V		–	0.5	2	–	4	
		V_{IN} = 1.05 V		–	0.4	1	–	3	
		V_{IN} = 0.6 V		–	0.2	1	–	2	
		V_{ON} = 0 V, V_{OUT} = 0 V,	3.3						μA
		V_{IN} = 3.3 V		–	0.8	3	–	7	
		V_{IN} = 2.5 V		–	0.6	2	–	5	
		V_{IN} = 1.8 V		–	0.5	2	–	4	
		V_{IN} = 1.05 V		–	0.3	1	–	3	
		V_{IN} = 0.6 V		–	0.2	1	–	2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. LOAD SWITCH RESISTANCE (Typical values are at T_A = +25°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	V_{BIAS} (V)	25°C			−40°C to 85°C	−40°C to 105°C	Unit
				Min	Typ	Max	Max	Max	
R_{ON}	On−State Resistance	V_{ON} = 5 V, I_{OUT} = −200 mA	5						mΩ
		V_{IN} = 5 V		–	3.9	4.8	5.7	6	
		V_{IN} = 3.3 V		–	3.9	4.8	5.7	6	
		V_{IN} = 2.5 V		–	3.9	4.8	5.7	6	
		V_{IN} = 1.8 V		–	3.9	4.8	5.7	6	
		V_{IN} = 1.05 V		–	3.9	4.8	5.7	6	
		V_{IN} = 0.6 V		–	3.9	4.8	5.7	6	
		V_{ON} = 5 V, I_{OUT} = −200 mA	3.3						mΩ
		V_{IN} = 3.3 V		–	3.9	4.8	5.7	6	
		V_{IN} = 2.5 V		–	3.9	4.8	5.7	6	
		V_{IN} = 1.8 V		–	3.9	4.8	5.7	6	
		V_{IN} = 1.05 V		–	3.9	4.8	5.7	6	
		V_{IN} = 0.6 V		–	3.9	4.8	5.7	6	

Table 7. OUTPUT PULL−DOWN RESISTANCE (NLPS22990 Only) (Typical values are at T_A = +25°C, unless otherwise noted.)

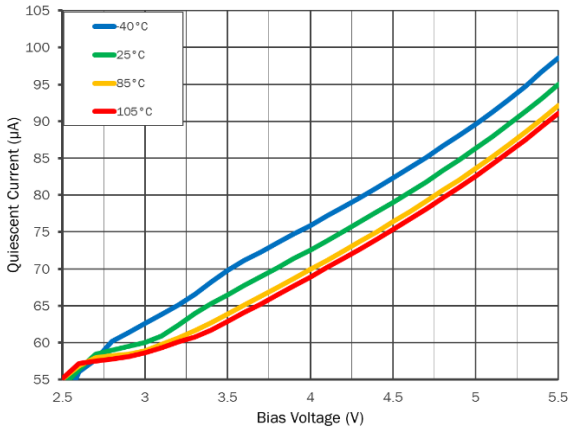
Symbol	Parameter	Test Conditions	V_{BIAS} (V)	−40°C to 105°C			Unit
				Min	Typ	Max	
R_{PD}	Output Pulldown Resistance	V_{ON} = 0 V, V_{IN} = V_{OUT} = 5 V	5	–	197	280	Ω
		V_{ON} = 0 V, V_{IN} = V_{OUT} = 3.3 V	3.3	–	204	280	

Table 8. SWITCHING CHARACTERISTICS (Typical values are at T_A = +25°C, unless otherwise noted.)

Symbol[4]	Parameter	Test Conditions	V_{BIAS} (V)	Min	Typ	Max	Unit
t_{ON}	Turn−On Time	V_{IN} = 5 V, V_{ON} = V_{BIAS}, R_L = 10 Ω, C_L = 0.1 μF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN} = 1 μF	5	–	24	–	μs
t_{OFF}	Turn−Off Time			–	6	–	
t_R	V_{OUT} Rise Time			–	31	–	
t_F	V_{OUT} Fall Time			–	2.9	–	
t_D	ON Delay Time			–	13	–	
$t_{PG,ON}$	PG Turn−On Time			–	119	–	
$t_{PG,OFF}$	PG Turn−Off Time			–	0.15	–	
t_{ON}	Turn−On Time	V_{IN} = 1.05 V, V_{ON} = V_{BIAS}, R_L = 10 Ω, C_L = 0.1 μF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN} = 1 μF	5	–	23	–	μs
t_{OFF}	Turn−Off Time			–	12	–	
t_R	V_{OUT} Rise Time			–	16	–	
t_F	V_{OUT} Fall Time			–	4.0	–	
t_D	ON Delay Time			–	16	–	
$t_{PG,ON}$	PG Turn−On Time			–	97	–	
$t_{PG,OFF}$	PG Turn−Off Time			–	0.15	–	
t_{ON}	Turn−On Time	V_{IN} = 0.6 V, V_{ON} = V_{BIAS}, R_L = 10 Ω, C_L = 0.1 μF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN} = 1 μF	5	–	24	–	μs
t_{OFF}	Turn−Off Time			–	13.5	–	
t_R	V_{OUT} Rise Time			–	11.7	–	
t_F	V_{OUT} Fall Time			–	3.8	–	
t_D	ON Delay Time			–	18	–	
$t_{PG,ON}$	PG Turn−On Time			–	95	–	
$t_{PG,OFF}$	PG Turn−Off Time			–	0.15	–	
t_{ON}	Turn−On Time	V_{IN} = 3.3 V, V_{ON} = 5 V, R_L = 10 Ω, C_L = 0.1 μF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN} = 1 μF	3.3	–	29	–	μs
t_{OFF}	Turn−Off Time			–	7.4	–	
t_R	V_{OUT} Rise Time			–	29	–	
t_F	V_{OUT} Fall Time			–	3.3	–	
t_D	ON Delay Time			–	18	–	
$t_{PG,ON}$	PG Turn−On Time			–	112	–	
$t_{PG,OFF}$	PG Turn−Off Time			–	0.21	–	
t_{ON}	Turn−On Time	V_{IN} = 1.05 V, V_{ON} = 5 V, R_L = 10 Ω, C_L = 0.1 μF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN} = 1 μF	3.3	–	30	–	μs
t_{OFF}	Turn−Off Time			–	11	–	
t_R	V_{OUT} Rise Time			–	18.5	–	
t_F	V_{OUT} Fall Time			–	4.0	–	
t_D	ON Delay Time			–	22	–	
$t_{PG,ON}$	PG Turn−On Time			–	101	–	
$t_{PG,OFF}$	PG Turn−Off Time			–	0.21	–	
t_{ON}	Turn−On Time	V_{IN} = 0.6 V, V_{ON} = 5 V, R_L = 10 Ω, C_L = 0.1 μF, C_T = 0 pF, R_{PU} = 10 kΩ, C_{IN} = 1 μF	3.3	–	31	–	μs
t_{OFF}	Turn−Off Time			–	13	–	
t_R	V_{OUT} Rise Time			–	14	–	
t_F	V_{OUT} Fall Time			–	3.8	–	
t_D	ON Delay Time			–	25	–	
$t_{PG,ON}$	PG Turn−On Time			–	99	–	
$t_{PG,OFF}$	PG Turn−Off Time			–	0.21	–	

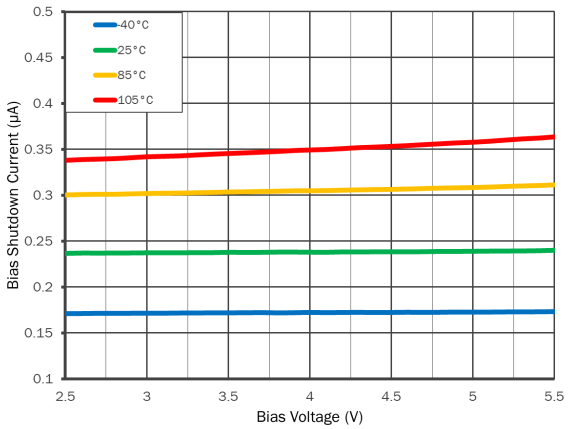
5. Turn−off time and fall time are dependent on the time constant at the load. For NLPS22990N, there is no QOD. The time constant is $R_L \times C_L$. For NLPS22990, internal pull down R_{PD} is enabled when the switch is disabled. The time constant is $(R_{PD}//R_L) \times C_L$.

Typical Characteristics



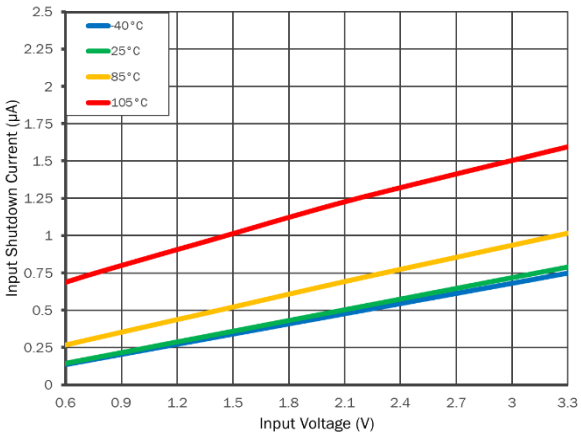
V_{ON} = 5 V, I_{OUT} = 0 A,V_{IN} = V_{BIAS}

Figure 5. Quiescent Current vs. Bias Voltage



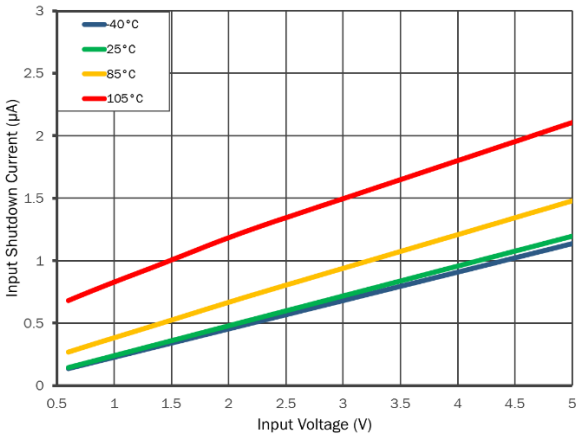
V_{ON} = 0 V, V_{OUT} = 0 V,V_{IN} = V_{BIAS}

Figure 6. Bias Shutdown Current vs. Bias Voltage



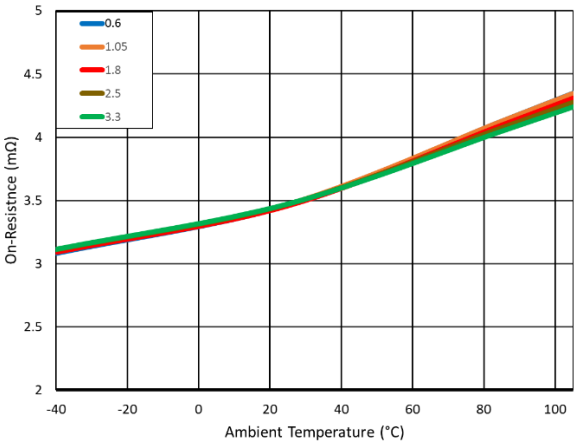
V_{ON} = 0 V, V_{BIAS} = 3.3 V,V_{OUT} = 0 V

Figure 7. Input Shutdown Current vs. Input Voltage



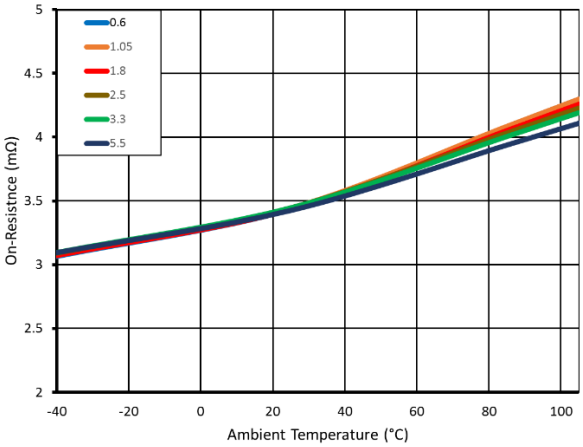
V_{ON} = 0 V, V_{BIAS} = 5 V,V_{OUT} = 0 V

Figure 8. Input Shutdown Current vs. Input Voltage



V_{ON} = 5 V, V_{BIAS} = 3.3 V, I_{OUT} = -200 mA

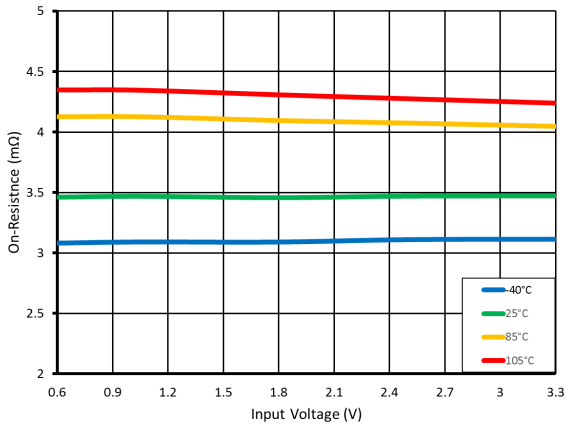
Figure 9. On−Resistance vs. Ambient Temperature



V_{ON} = 5 V, V_{BIAS} = 5 V, I_{OUT} = -200 mA

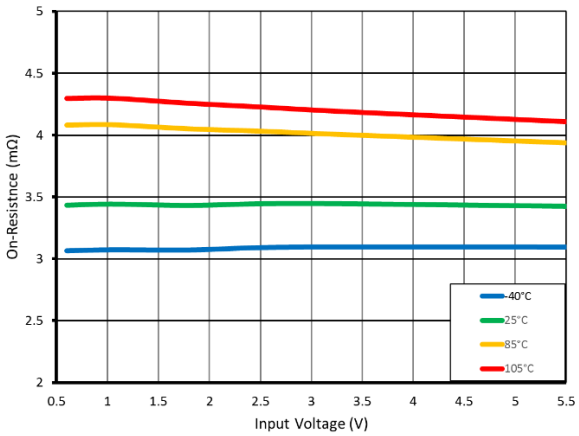
Figure 10. On−Resistance vs. Ambient Temperature

Typical Characteristics



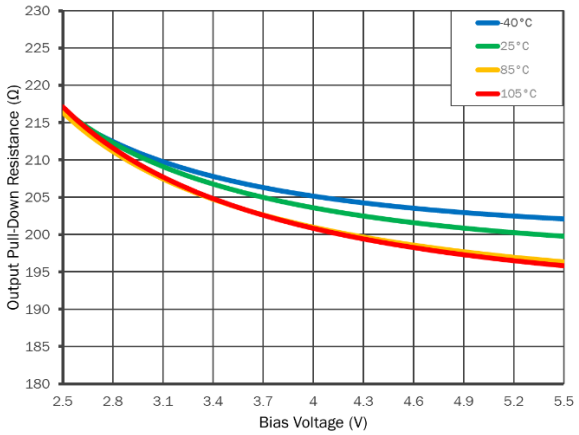
V_{ON} = 5 V, V_{BIAS} = 3.3 V, I_{OUT} = -200 mA

Figure 11. On−Resistance vs. Input Voltage



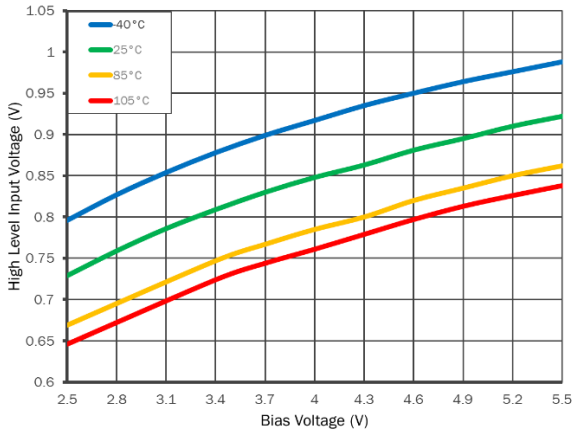
V_{ON} = 5 V, V_{BIAS} = 5 V, I_{OUT} = -200 mA

Figure 12. On−Resistance vs. Input Voltage



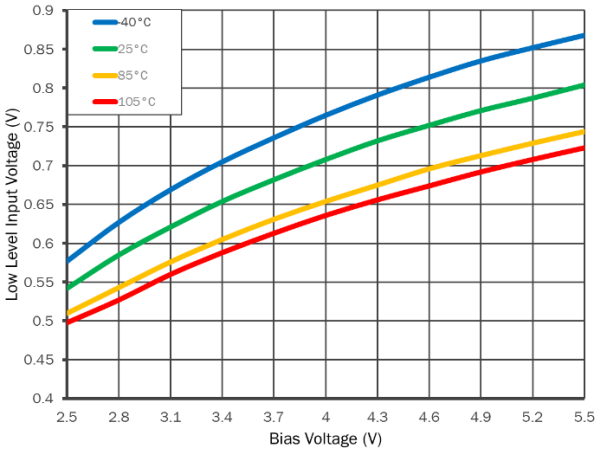
V_{ON} = 0 V, V_{OUT} = V_{IN} = 1.05 V

Figure 13. Output Pull−Down Resistance vs. Bias Voltage



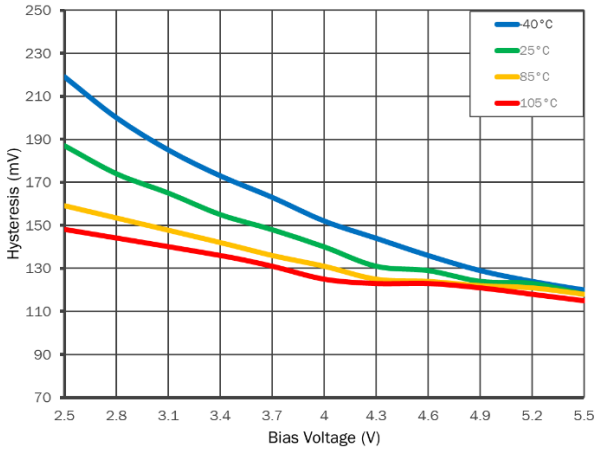
I_{OUT} = 0 A

Figure 14. High−Level Input Voltage vs. Bias Voltage



I_{OUT} = 0 A

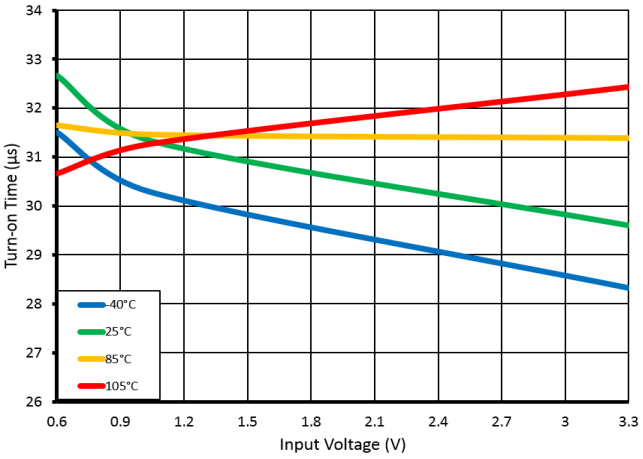
Figure 15. Low−Level Input Voltage vs. Bias Voltage



I_{OUT} = 0 A

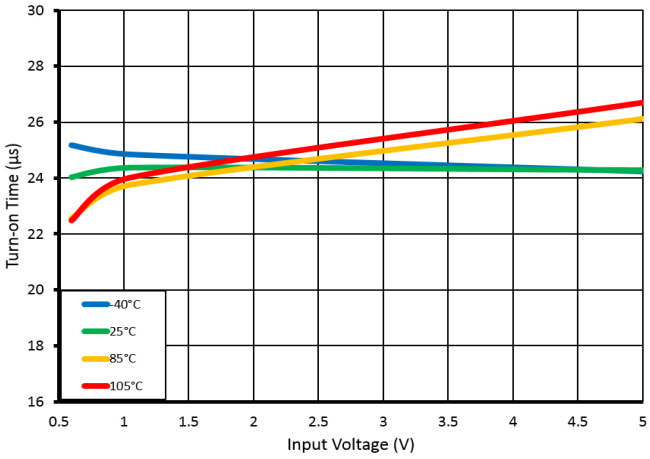
Figure 16. Hysteresis vs. Bias Voltage

Typical Characteristics



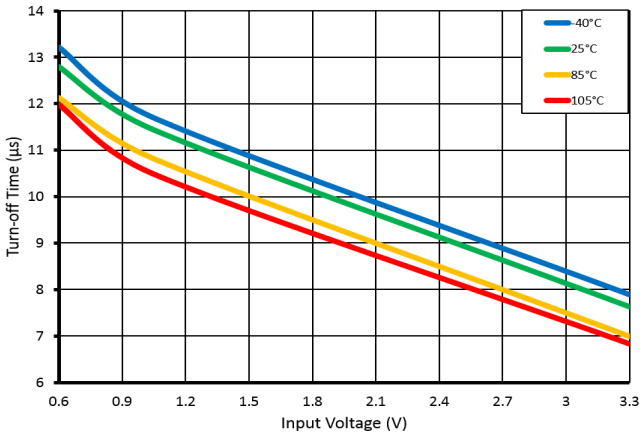
V_{BIAS} = 3.3 V, V_{ON} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 17. Turn−on Time vs. Input Voltage



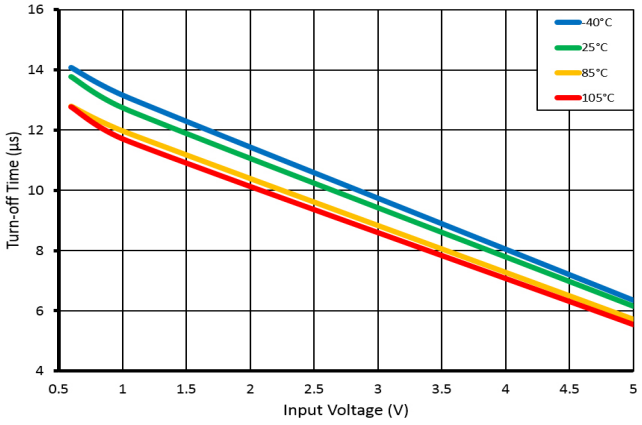
V_{BIAS} = 5 V, V_{ON} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 18. Turn−on Time vs. Input Voltage



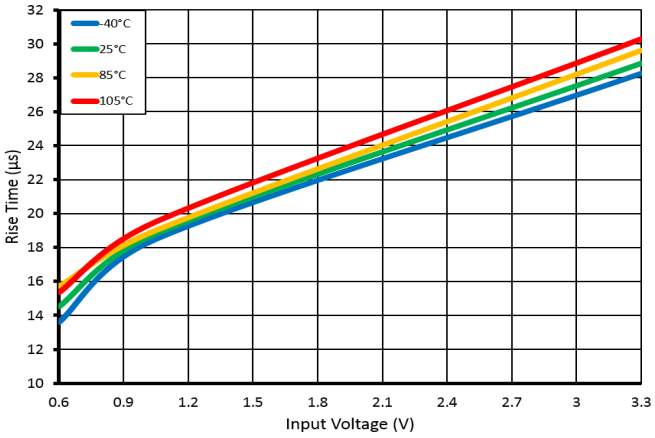
V_{BIAS} = 3.3 V, V_{ON} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 19. Turn−off Time vs. Input Voltage



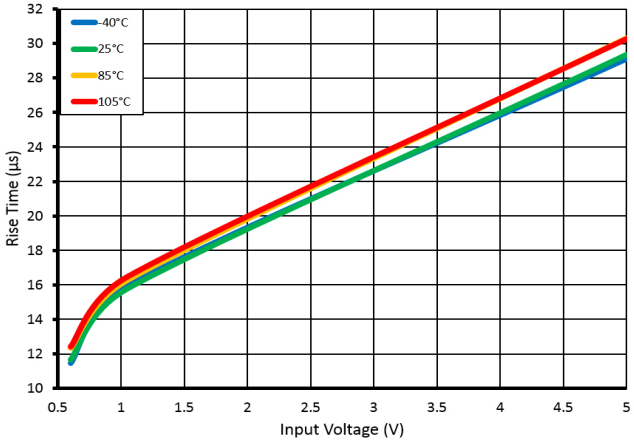
V_{BIAS} = 5 V, V_{ON} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 20. Turn−off Time vs. Input Voltage



V_{BIAS} = 3.3 V, V_{ON} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

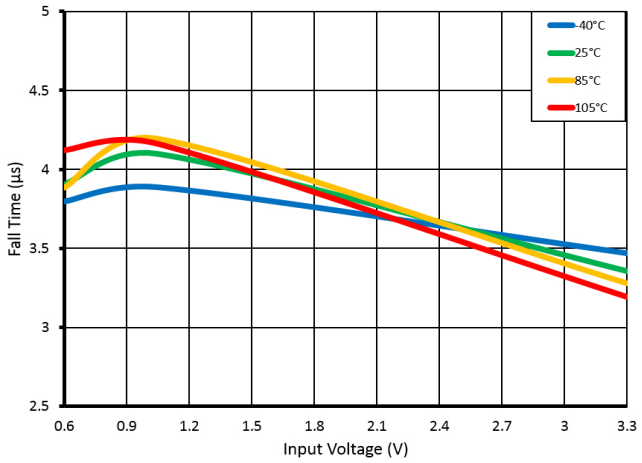
Figure 21. Rise Time vs. Input Voltage



V_{BIAS} = 5 V, V_{ON} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

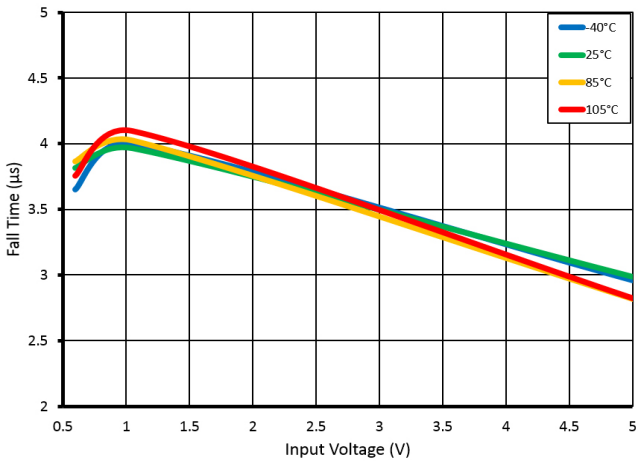
Figure 22. Rise Time vs. Input Voltage

Typical Characteristics



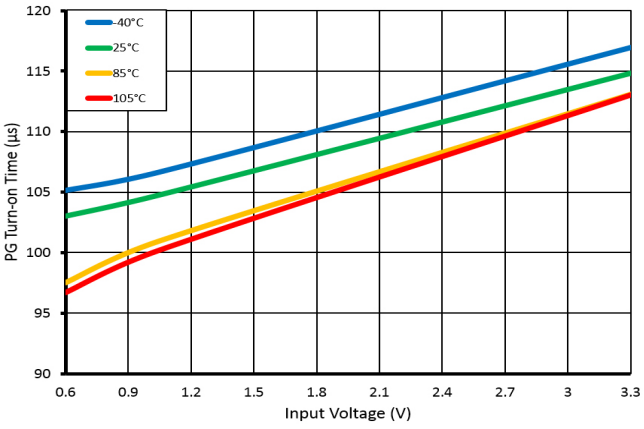
V_{BIAS} = 3.3 V, V_{ON} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 23. Fall Time vs. Input Voltage



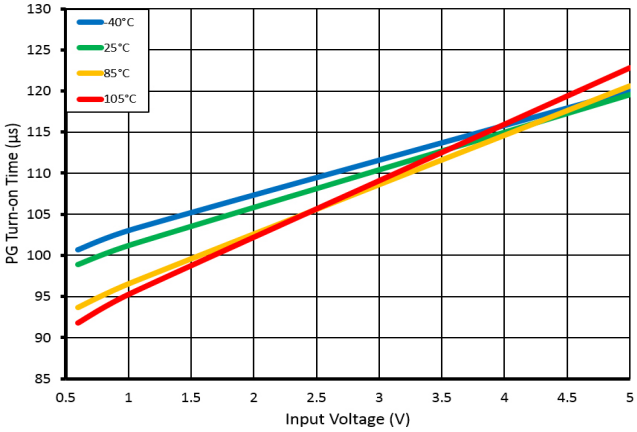
V_{BIAS} = 5 V, V_{ON} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 24. Fall Time vs. Input Voltage



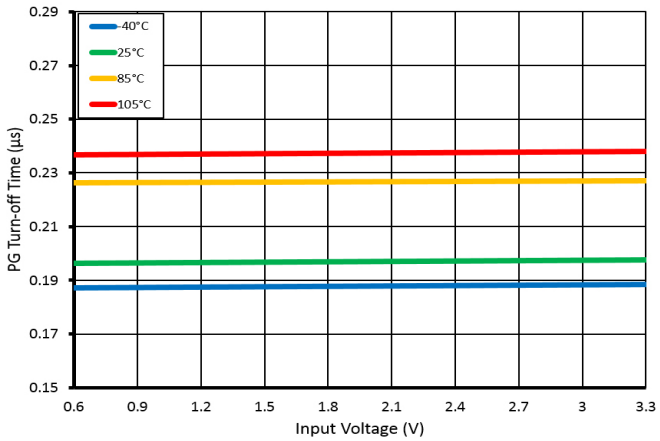
V_{BIAS} = 3.3 V, V_{ON} = 5 V, C_T = 0 pF,
R_{PU} = 10 kΩ, C_L = 0.1 µF, R_L = 10 Ω

Figure 25. PG Turn−on Time vs. Input Voltage



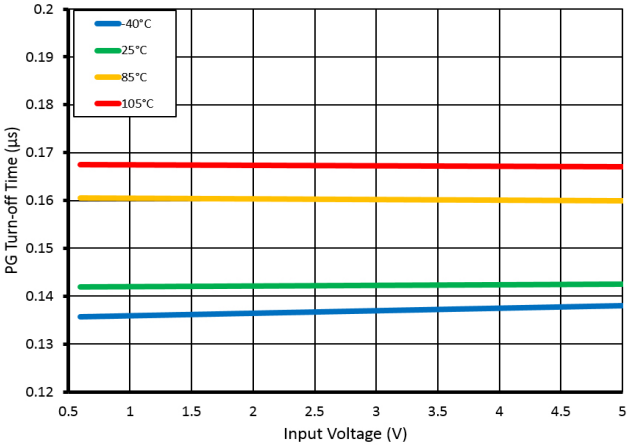
V_{BIAS} = 5 V, V_{ON} = 5 V, C_T = 0 pF,
R_{PU} = 10 kΩ, C_L = 0.1 µF, R_L = 10 Ω

Figure 26. PG Turn−on Time vs. Input Voltage



V_{BIAS} = 3.3 V, V_{ON} = 5 V, C_T = 0 pF,
R_{PU} = 10 kΩ, C_L = 0.1 µF, R_L = 10 Ω

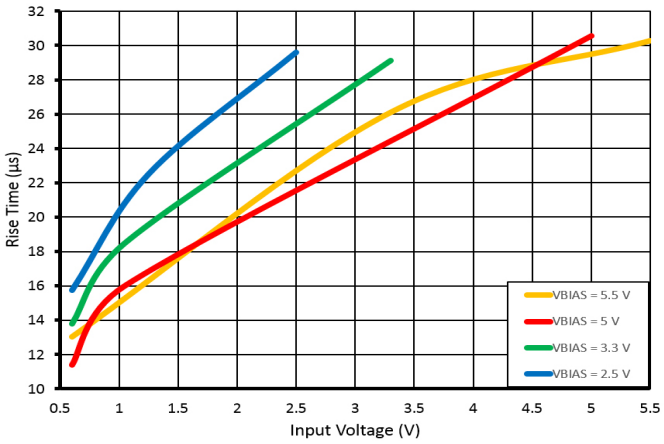
Figure 27. PG Turn−off vs. Input Voltage



V_{BIAS} = 5 V, V_{ON} = 5 V, C_T = 0 pF,
R_{PU} = 10 kΩ, C_L = 0.1 µF, R_L = 10 Ω

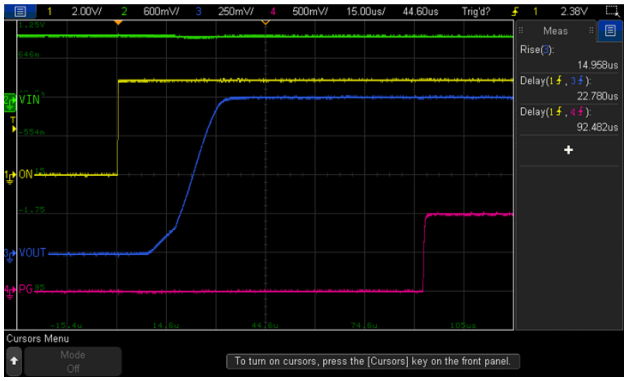
Figure 28. PG Turn−off Time vs. Input Voltage

Typical Characteristics



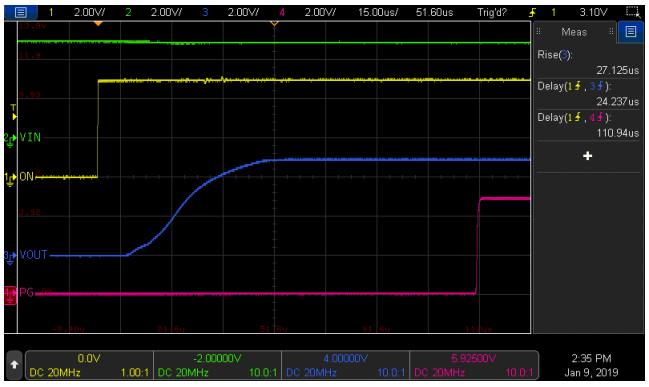
T_A = 25 °C, C_L = 0.1 µF, C_T = 0 pF,
C_{IN} = 1 µF, R_L = 10 Ω

Figure 29. Rise Time vs. Input Voltage



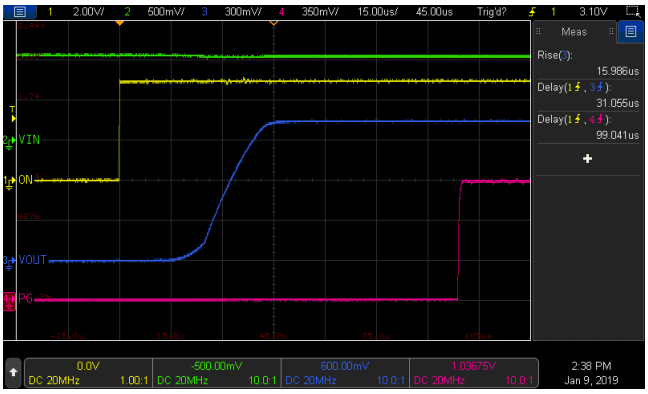
V_{BIAS} = 5 V, V_{IN} = 1.05 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 30. Turn−on Response



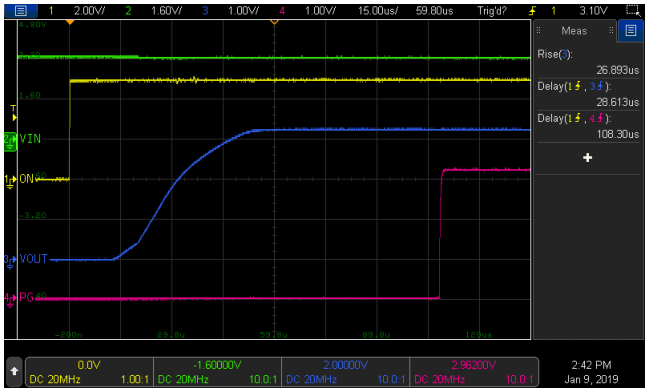
V_{BIAS} = 5 V, V_{IN} = 5 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 31. Turn−on Response



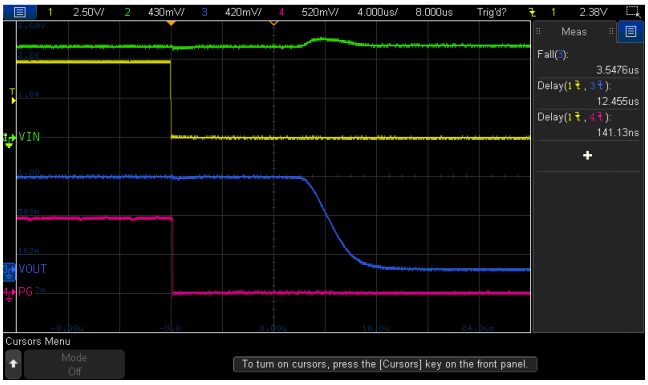
V_{BIAS} = 3.3 V, V_{IN} = 1.05 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

Figure 32. Turn−on Response



V_{BIAS} = 3.3 V, V_{IN} = 3.3 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

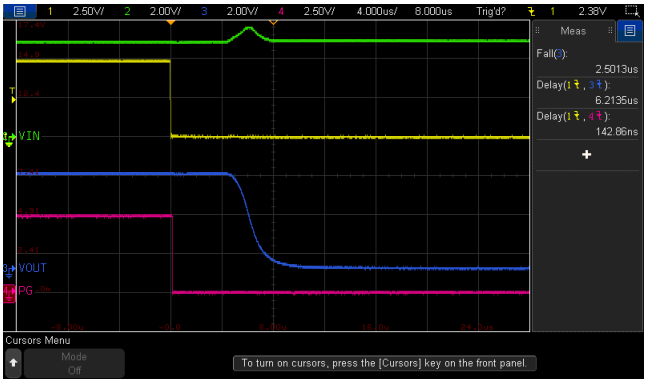
Figure 33. Turn−on Response



V_{BIAS} = 5 V, V_{IN} = 1.05 V, C_T = 0 pF,
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

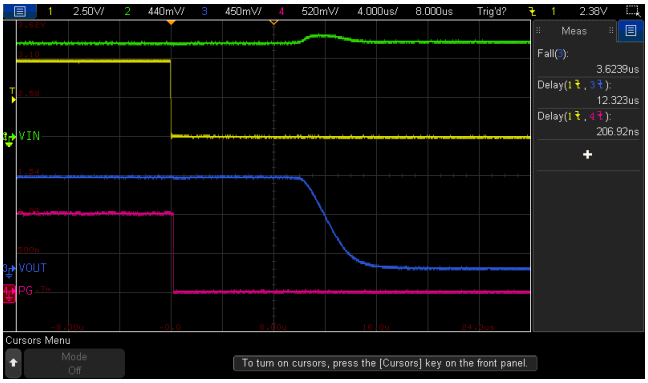
Figure 34. Turn−on Response

Typical Characteristics



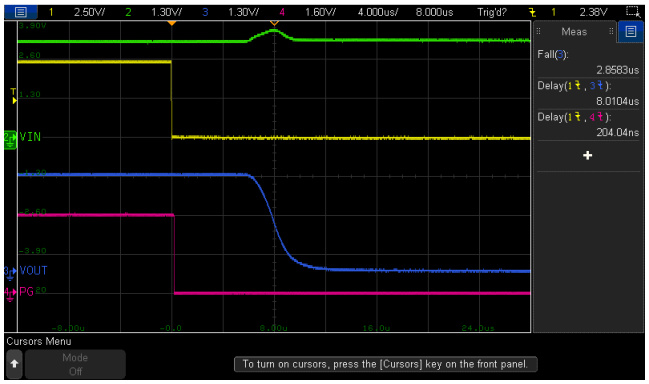
V_{BIAS} = 5 V, V_{IN} = 5 V, C_T = 0 pF,
C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω

Figure 35. Turn−off Response



V_{BIAS} = 3.3 V, V_{IN} = 1.05 V, C_T = 0 pF,
C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω

Figure 36. Turn−off Response



V_{BIAS} = 3.3 V, V_{IN} = 3.3 V, C_T = 0 pF,
C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω

Figure 37. Turn−off Response

Parameter Measurement Information

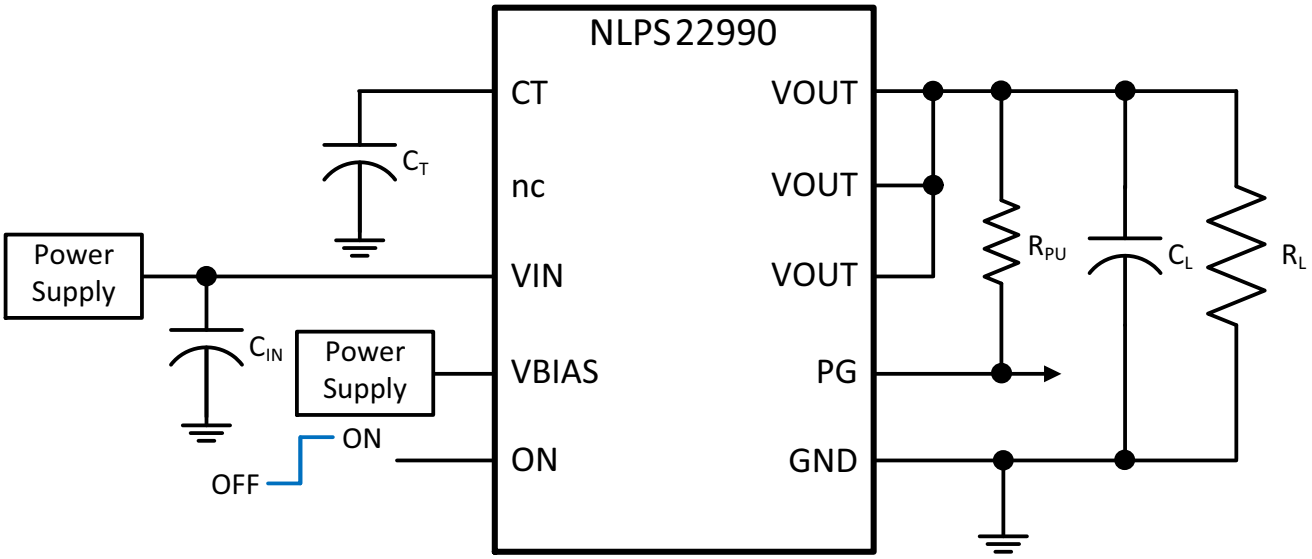
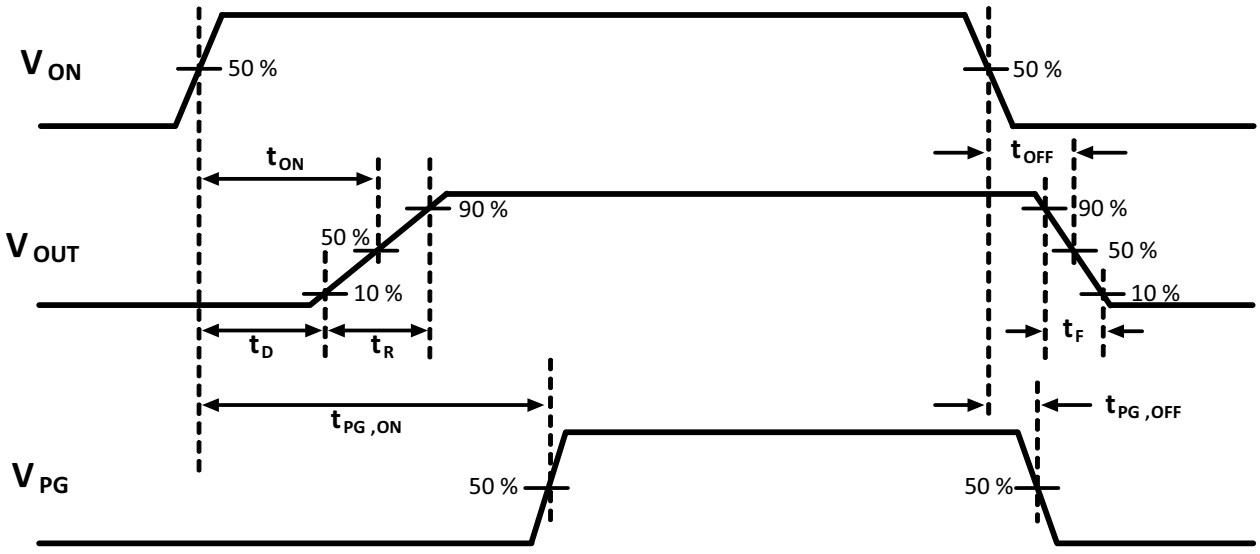


Figure 38. Timing Test Circuit



Rise/fall time of the control signals is 100 ns.

Figure 39. Timing Waveforms

Detailed Description

Overview

The NLPS22990 / NLPS22990N device is a single channel load switch with controlled adjustable turn−on time and an integrated PG indicator. The device contains an N−channel MOSFET that can operate over an input voltage range of 0.6 V to 5.5 V and can support a maximum continuous current of 10 A. The wide input voltage range and high current capability enable this device to be used across multiple designs and end equipment. The on−resistance of 3.9−mΩ minimizes the voltage drop across the load switch and the power loss due to the load switch.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. Adjustable slew rate through the CT pin provides design flexibility in trading off inrush current and power up timing requirements. The integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing. During shutdown, the device has very low leakage current, thereby reducing unnecessary leakages for downstream modules during standby. The NLPS22990 features an internal 200−Ω resistor for quick discharge of the output when switch is disabled. The NLPS22990N does not have this quick output discharge feature.

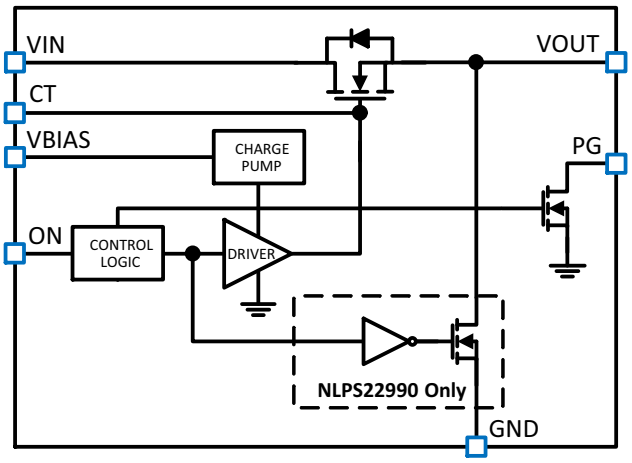


Figure 40. Functional Block Diagram

Feature Description

On and Off Control

The ON pin controls the state of the load switch. Asserting the pin high enables the switch. The minimum voltage that guarantees logic high is 1.0 V. This pin cannot be left floating and must be tied either high or low for proper functionality.

Adjustable Rise Time

The NLPS22990 / NLPS22990N features adjustable rise time for inrush current control. A capacitor to GND on the CT pin adjusts the rise time. Without any capacitor on the CT, the rise time is at its minimum for fastest timing. The voltage on the CT pin can be as high as 15 V; therefore the minimum voltage rating for the CT capacitor must be 25 V for optimal performance. An approximate equation for the relationship between CT, V_{IN} and rise time when V_{BIAS} is set to 5 V is shown in Equation 1. As shown in Figure 39, rise time is defined as from 10% to 90% measurement on V_{OUT}.

$$t_R = (0.0058 \times V_{IN} + 0.0005) \times C_T + 5.4 \times V_{IN} + 2.8 \quad \text{(eq. 1)}$$

where

- t_R is the rise time (in μs)
- V_{IN} is the input voltage (in V)
- C_T is the capacitance value on the CT pin (in pF)

Table 9 contains rise time values measured on a typical device. Rise times shown below are only valid for the power−up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON pin is asserted high.

Table 9. RISE TIME VS. CT CAPACITOR

	Rise Time (μs) at 25°C, C_L = 0.1 uF, C_{IN} = 1 uF, R_L = 10 Ω, V_{BIAS} = 5 V				
C_T (pF)	V_{IN} = 5 V	V_{IN} = 3.3 V	V_{IN} = 1.8 V	V_{IN} = 1.05 V	V_{IN} = 0.6 V
0	26.4	23.5	19.6	14.2	10.7
220	30.5	26.2	21.4	14.6	11.0
470	36.6	29.4	21.7	16.0	12.2
1000	52.9	40.6	28.1	20.7	14.9
2200	86.6	63.7	41.7	29.0	20.1
4700	160.5	112.0	70.6	46.9	32.7
10000	310.8	214.1	130.4	84.0	56.4

Power Good (PG)

The NLPS22990 / NLPS22990N has a power good (PG) output signal used to indicate that the gate of the pass FET is driven high, and that the switch is on with On−resistance close to its final value (full load ready). PG is an active high open−drain output which can be connected to a voltage source through an external pull up resistor, R_{PU}. This voltage source can be V_{OUT} from the NLPS22990 / NLPS22990N or another external voltage. V_{BIAS} is required for PG to have a valid output. Equation 2 shows the approximate equation for the relationship between CT, V_{IN} and PG turn−on time ($t_{PG,ON}$) when V_{BIAS} is set to 5 V.

(eq. 2)

$$t_{PG,ON} = (0.0083 \times V_{IN} + 0.023) \times C_T + 4.4 \times V_{IN} + 85$$

where

- $t_{PG,ON}$ is the PG turn−on time (in μs)
- V_{IN} is the input voltage (in V)
- C_T is the capacitance value on the CT pin (in pF)

Table 10 contains PG turn−on time values measured on a typical device.

Table 10. PG TURN−ON TIME VS. CT CAPACITOR

	Typical PG Turn−on Time (μs) at 25°C C_L = 0.1 uF, C_{IN} = 1 uF, R_L = 10 Ω, V_{BIAS} = 5 V				
C_T (pF)	**V_{IN} = 5 V**	**V_{IN} = 3.3 V**	**V_{IN} = 1.8 V**	**V_{IN} = 1.05 V**	**V_{IN} = 0.6 V**
0	110.86	101.19	95.5	92.01	91.68
220	125.05	112.49	104.0	99.84	97.7
470	140.84	125.02	114.01	108.67	104.53
1000	174.71	151.86	134.84	126.33	120.87
2200	249.15	210.8	179.5	164.72	155.37
4700	408.76	335.95	276.0	246.93	229.46
10000	734.93	594.64	474.98	415.5	380.43

Quick Output Discharge (QOD) (NLPS22990 Only)

The NLPS22990 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between V_{OUT} and GND. This resistor has a typical value of 200 Ω and prevents the output from floating while the switch is disabled.

The NLPS22990N does not have this feature.

Table 11. FUNCTION TABLE

ON	**V_{IN} to V_{OUT}**	**OUTPUT DISCHARGE** (Note 6)
L	OFF	ENABLED
H	ON	DISABLED

6. This feature is in the NLPS22990 only (not in NLPS22990N).

Device Functional Modes

Table 11 shows the function table for NLPS22990.

Application and Implementation

Application Information

Input to Output Voltage Drop

The input to output voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. See the R_{ON} specifications in the Resistance Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 3 to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \quad \text{(eq. 3)}$$

where

- ΔV is the voltage drop from V_{IN} to V_{OUT}
- I_{LOAD} is the load current
- R_{ON} is the on−resistance of the device for a specific V_{IN} and V_{BIAS}
- An appropriate I_{LOAD} must be chosen such that the IMAX specification of the device is not violated

Input Capacitor

The use of a capacitor between V_{IN} and GND close to these pins is recommended. This helps limit the voltage drop on the input supply caused by transient inrush currents into a discharged capacitor at the load when the switch is turned on. A 1−μF ceramic capacitor, C_{IN}, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup. C_L refers to the load capacitance.

Thermal Consideration

The maximum junction temperature should be limited below 125°C. Use Equation 4 to calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output load current and ambient temperature. $R_{\theta JA}$ is highly dependent upon board layout.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{(eq. 4)}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation
- $T_{J(max)}$ is the maximum allowable junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the junction−to−air thermal impedance

PG Pull Up Resistor

PG is an open−drain output which should be connected to a voltage source through a pull up resistor R_{PU}. The PG signal can be used to drive the enable pins of downstream devices, EN. PG is active high, and its voltage is given by Equation 5.

$$V_{PG} = V_{OUT} - (I_{PG,LK} + I_{EN,LK}) \times R_{PU} \quad \text{(eq. 5)}$$

where

- V_{OUT} is the voltage where PG is tied to
- $I_{PG,LK}$ is the leakage current into PG pin
- $I_{EN,LK}$ is the leakage current into the EN pin driven by PG
- R_{PU} is the pull up resistance

V_{PG} needs to be higher than $V_{IH,MIN}$ of the EN pin to be interpreted as a valid logic high. The maximum R_{PU} is determined by Equation 6.

$$R_{PU,MAX} = \frac{V_{OUT} - V_{IH,MIN}}{I_{PG,LK} + I_{EN,LK}} \quad \text{(eq. 6)}$$

When PG is disabled, a 1 mA current into PG pin (I_{PG} = 1 mA) produces a $V_{PG,OL}$ of less than 0.2 V. This $V_{PG,OL}$ will be interpreted as a valid logic low as long as $V_{IL,MAX}$ of the EN pin is greater than 0.2 V. The minimum R_{PU} is determined by Equation 7.

$$R_{PU,MIN} = \frac{V_{OUT}}{I_{PG} + I_{EN,LK}} \quad \text{(eq. 7)}$$

R_{PU} can be chosen within the range defined by $R_{PU,MIN}$ and $R_{PU,MAX}$. R_{PU} = 10 kΩ is used for characterization.

Power Sequencing

The NLPS22990 / NLPS22990N has an integrated power good indicator which can be used for power sequencing. As shown in Figure 41, the switch to the second load is controlled by the PG signal from the first switch. This ensures that the power to load 2 is only enabled after the power to load 1 is enabled and the first switch is full−load ready.

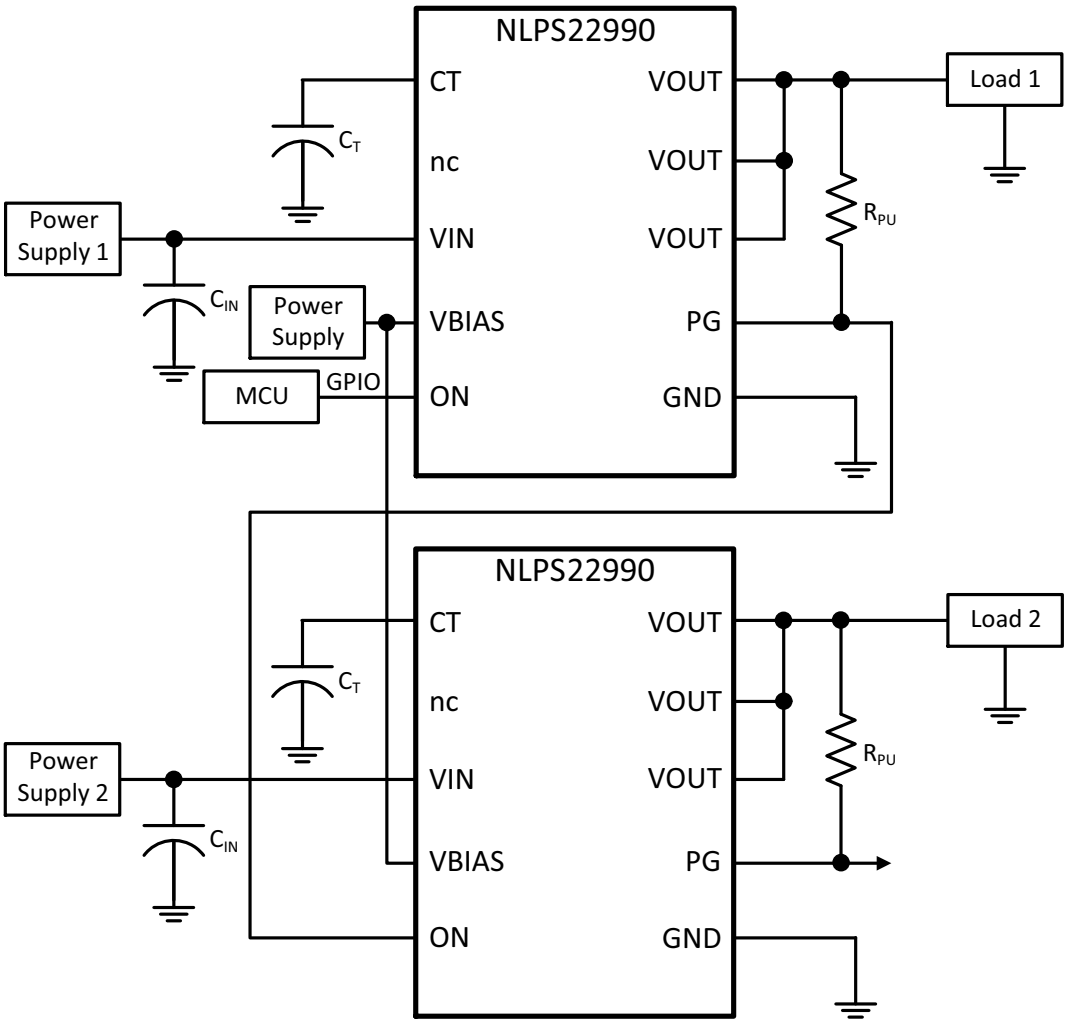


Figure 41. Power Sequencing

Standby Power Reduction

Any end equipment that is powered by a battery sees the need to reduce current consumption in order to maintain the battery charge for a longer time. The NLPS22990 / NLPS22990 devices help to accomplish this reduction by turning off the supply to the downstream modules that are in standby state. Turning off the supply significantly reduces the leakage current overhead of the standby modules as shown in Figure 42.

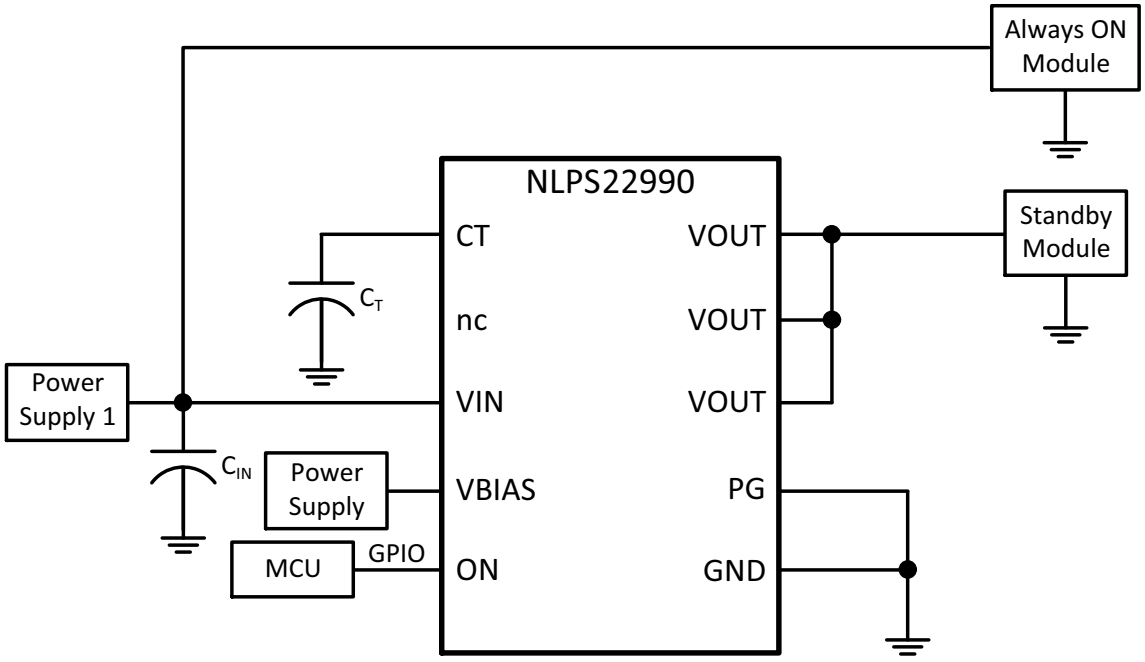


Figure 42. Standby Power Reduction

Power Supply Recommendations

The device is designed to operate with a V_{BIAS} range of 2.5 V to 5.5 V, and a V_{IN} range of 0.6 V to V_{BIAS}. The supply must be well regulated and placed as close to the device terminal as possible with the recommended 1−μF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. In the case where the power supply is slow to respond to a large load current step, additional bulk may also be required. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 μF may be sufficient.

Layout

Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects. The C_T trace must be as short as possible to reduce parasitic capacitance.

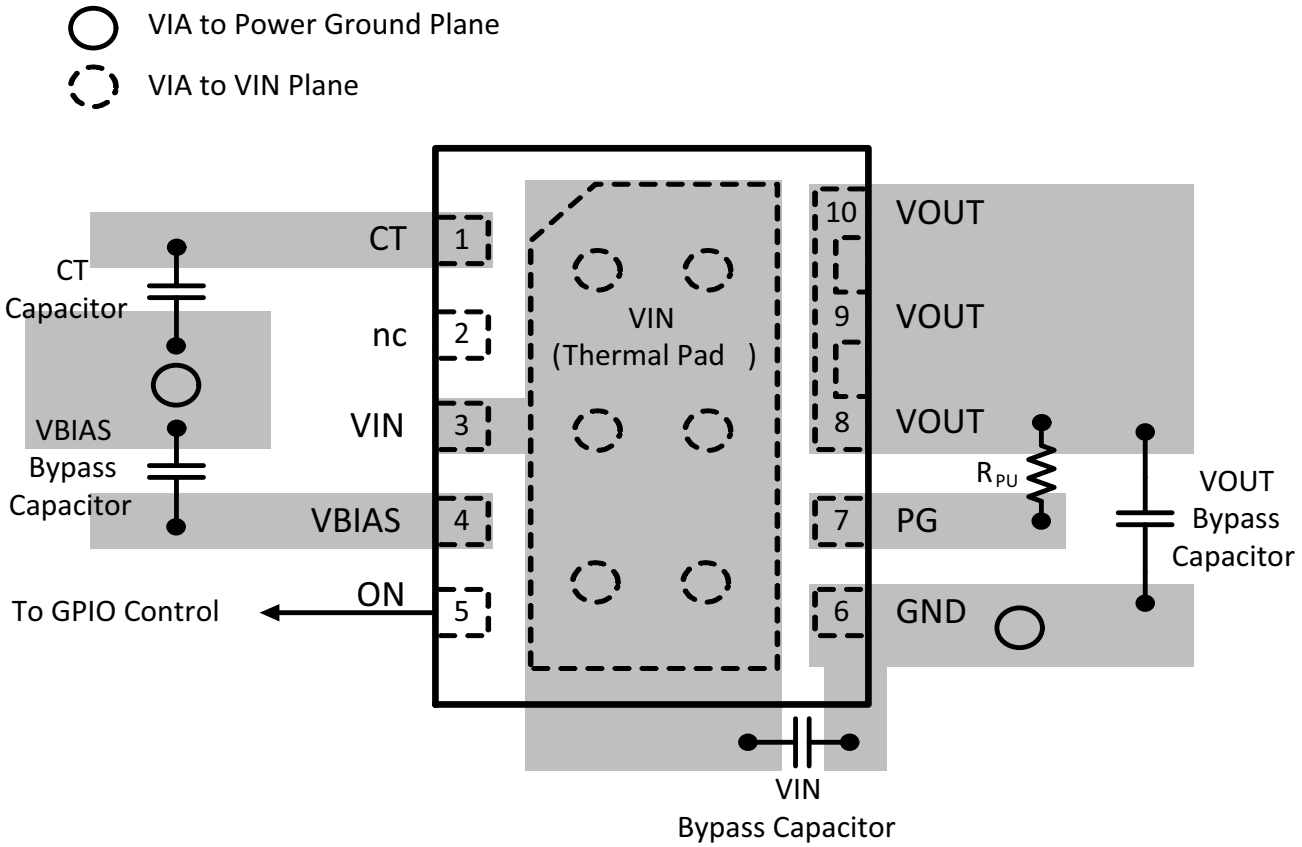
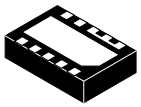


Figure 43. Layout Example

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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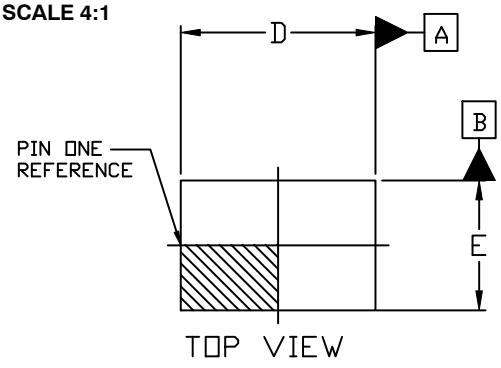
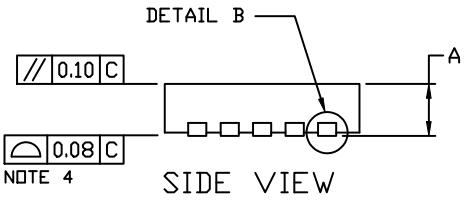
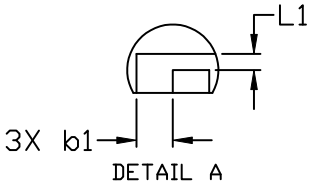
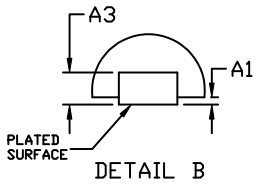
WDFN10 3.0x2.0, 0.5P
CASE 511DX
ISSUE A

DATE 15 NOV 2018



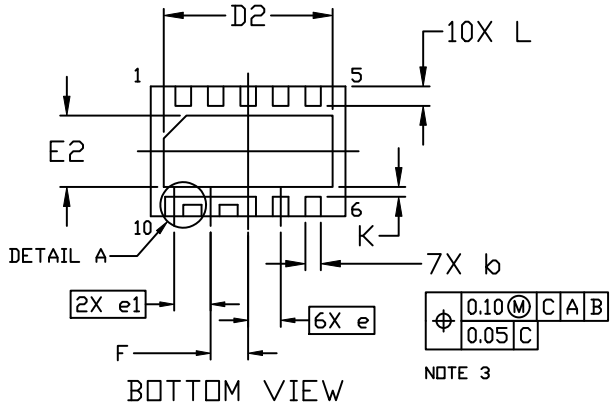


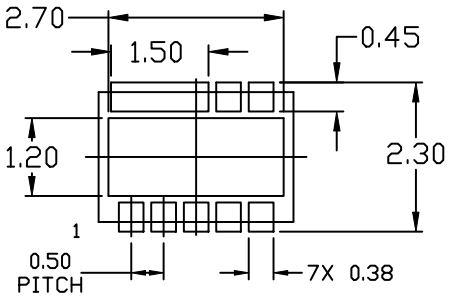




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b, b1 AND b2 APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM THE TERMINAL TIP.
4. PROFILE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
b	0.19	0.24	0.29
b1	0.23	0.28	0.33
D	2.90	3.00	3.10
D2	2.50	2.60	2.70
E	1.90	2.00	2.10
E2	1.00	1.10	1.20
e		0.50 BSC	
e1		0.56 BSC	
F		0.58 REF	
k		0.15 REF	
L	0.25	0.30	0.35
L1		0.125 REF	

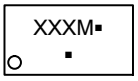




RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN10 3.0x2.0, 0.5P**	**PAGE 1 OF 1**

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