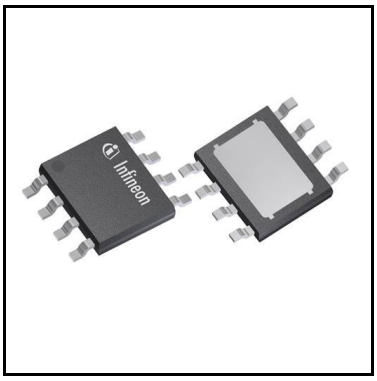
HITFET^{TM}+ 24V

BTT3018EJ Smart Low-Side Power Switch



Features

- Single channel device optimized for 24 V applications
- Electrostatic discharge protection (ESD)
- Over current, active clamping and over temperature protection
- Over temperature latch shutdown
- Supply pin undervoltage protection
- Dedicated status signal
- Slew-rate control to adjust switching speed
- PWM switching capability of 20KHz (duty cycle 10%-90%)
- Green Product (RoHS compliant)
- AEC Qualified

Potential applications

- Suitable for resistive and inductive loads

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The BTT3018EJ is a 16 mΩ single channel Smart Low-Side Power Switch within a PG-TDSO-8 package providing embedded protective functions. The power transistor is built by a N-channel vertical power MOSFET. The BTT3018EJ is monolithically integrated.
The BTT3018EJ is automotive qualified and is optimized for 24 V automotive applications.

Table 1 Product Summary

Parameter	Symbol	Values
Operating Voltage Range	V_{OUT}	0 … 36 V
Maximum load voltage	$V_{BAT(OUT)}$	63 V
ON-State Resistance	$R_{DS(ON)\_25}$	16 mΩ
Nominal Load Current	$I_{L(NOM)}$	7.0 A
Minimum Current Limitation	$I_{L(LIM)}$	30 A

Type	Package	Marking
BTT3018EJ	PG-TDSO-8	T3018EJ

Table of Contents

1 Block Diagram

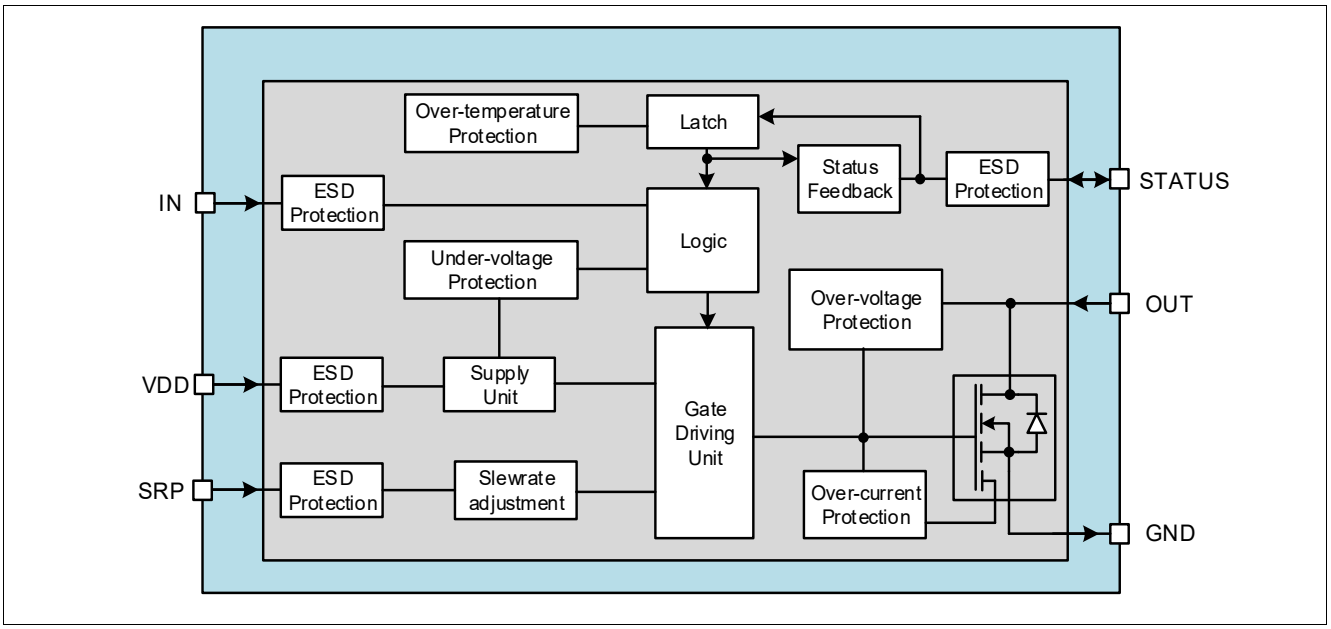


Figure 1 Block Diagram of the BTT3018EJ

2 Pin Configuration

2.1 Pin Assignment

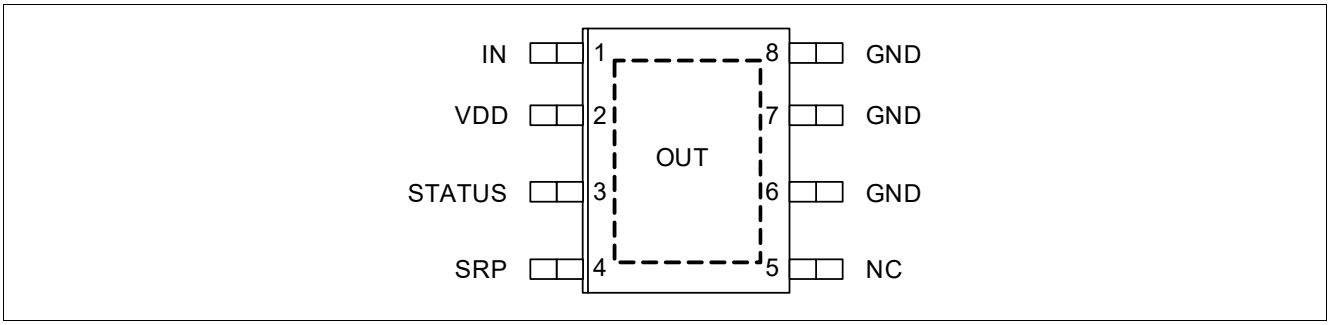


Figure 2 Pin Configuration. PG-TDSO-8

2.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1	IN	I	If IN is high, switches ON the Power DMOS If IN is low, switches OFF the Power DMOS
2	VDD	I	Logic supply voltage pin, 3.3V to 5.5V
3	STATUS	I/O	RESET thermal latch function by microcontroller and pull-up If STATUS is high, device is in normal operation If STATUS is low, device is in over temperature condition
4	SRP	I	Slewrate control with external resistor
5	NC		Pin internally not connected
6, 7, 8	GND	I/O	GND; Source of power DMOS and logic[1)]
Cooling Tab	OUT	I/O	Load connection, Drain of power DMOS

1) All GND pins must be connected together

2.3 Voltage and Current Definition

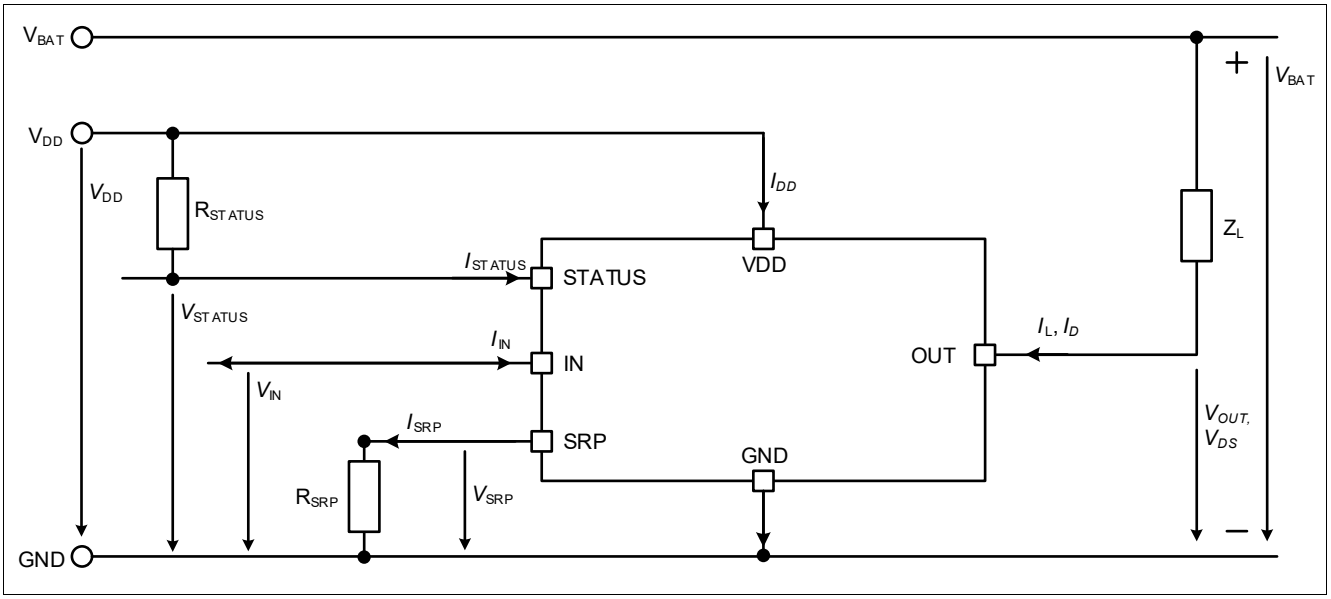


Figure 3 Naming definition of electrical parameters

3 General Product Characteristics

3.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Voltages							
Output Voltage	V_{OUT}	-0.3	–	63	V	internally clamped	P_3.1.1
Battery Voltage for short circuit protection (Extended Range)	$V_{BAT(SC)}$	-0.3	–	36	V	V_{IN} = 5V	P_3.1.2
Power Stage							
Load current	I_L	0	–	$I_{L(LIM)}$	A	–	P_3.1.3
Logic Pins							
IN Pin Voltage	V_{IN}	-0.3	–	5.5	V	–	P_3.1.4
STATUS Pin Voltage	V_{STATUS}	-0.3	–	5.5	V	–	P_3.1.5
SRP Pin Voltage	V_{SRP}	-0.3	–	5.5	V	–	P_3.1.6
VDD Pin Voltage	V_{DD}	-0.3	–	6.5	V	–	P_3.1.7
Energy capability							
Energy. Single pulse	E_{AS}	–	–	150	mJ	$I_{L(0)} = I_{L(NOM)}$ V_{BAT} = 28 V $T_{J(0)}$ = 150°C	P_3.1.8
Energy. Repetitive pulse 1 M cycles	$E_{AR(1M)}$	–	–	80	mJ	$I_{L(0)} = I_{L(NOM)}$ V_{BAT} = 28V $T_{J(0)}$ = 105°C	P_3.1.11
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_3.1.13
Storage Temperature	T_{STG}	-55	–	150	°C	–	P_3.1.14
ESD Susceptibility							
ESD Susceptibility (all pins except OUT tab, to GND)	V_{ESD}	-2	–	2	kV	HBM[2)]	P_3.1.15
ESD Susceptibility (OUT tab to GND)	V_{ESD_OUT}	-4	–	4	kV	HBM[2)]	P_3.1.16
ESD Susceptibility (all pins)	V_{ESD_CDMA}	-500	–	500	V	CDM[3)]	P_3.1.17
ESD Susceptibility (corner pins)	V_{ESD_CDMC}	-750	–	750	V	CDM[3)]	P_3.1.18

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF.)
3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional Range

Table 3 Functional Range [1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Battery Voltage Range for Nominal Operation	$V_{BAT(NOR)}$	6	–	36	V	–	P_3.2.1
Supply Voltage Range for Nominal Operation	$V_{DD(NOR)}$	3.3	–	5.5	V	–	P_3.2.2
Supply Voltage Range for Extended_1 Operation	$V_{DD(EXT1)}$	3.0	–	5.5	V	1) Parameter deviations possible	P_3.2.6
Battery Voltage Range for Extended_2 Operation	$V_{DD(EXT2)}$	5.5	–	6.5	V	1) V_{BAT} < 46V; Parameter deviations possible	P_3.2.7
Junction Temperature	T_J	-40	–	150	°C	–	P_3.2.4
External Resistor Range for Adjustable Slewrate Operation	R_{SRP}	2.2	–	160	kΩ	–	P_3.2.5

1) Not subject to production test, specified by design.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	0.84	–	K/W	1) 2)	P_3.3.1
Junction to Ambient 2s2p	$R_{thJA(2s2p)}$	–	30	–	K/W	1) 3)	P_3.3.2

1) Not subject to production test, specified by design.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup. Bottom of the package is fixed to ambient temperature. T_{AMB} = 85°C. Device loaded with 1 W power

3) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). T_{AMB} = 85°C. Device loaded with 1 W power

3.4 Transient Thermal Impedance

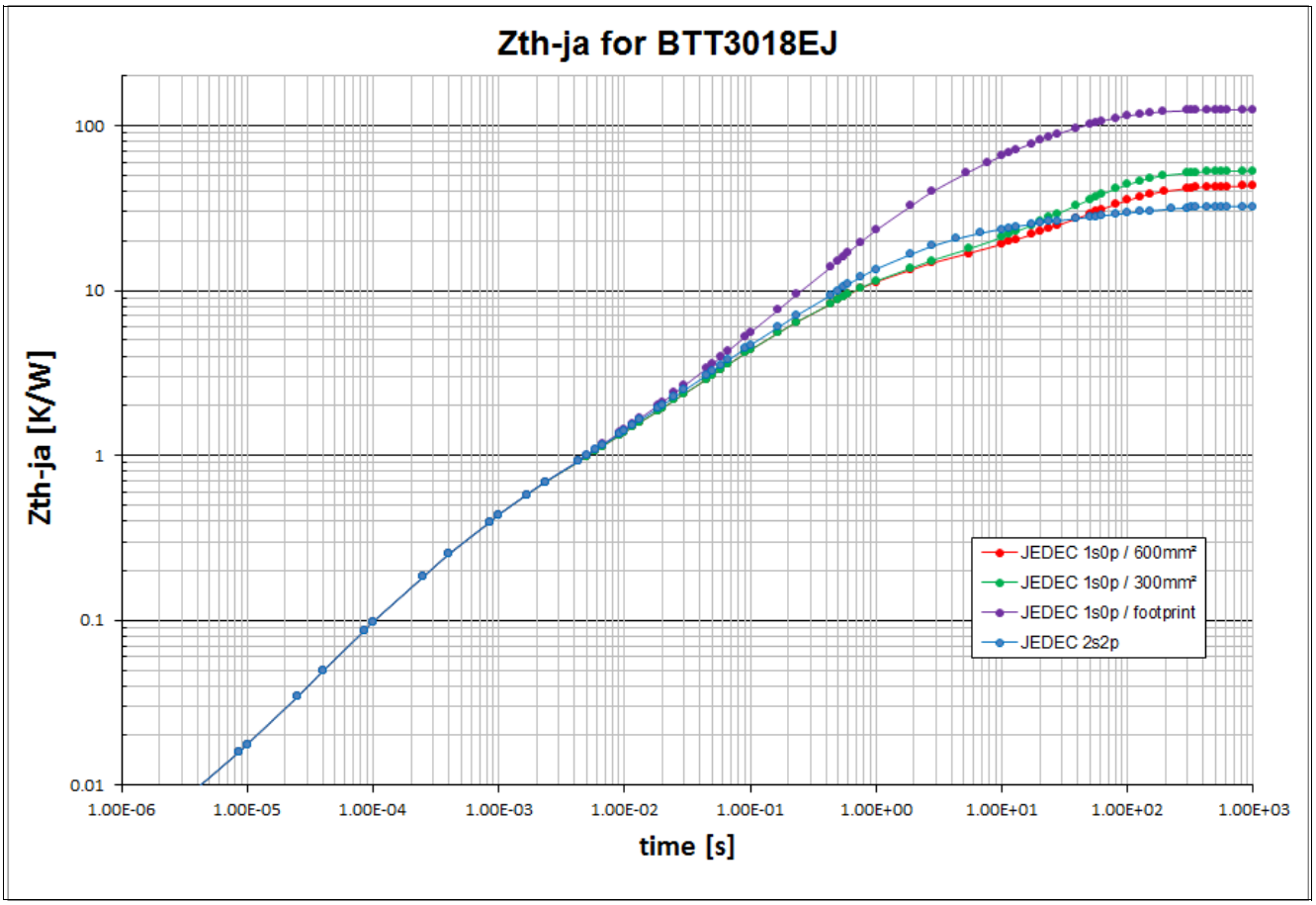


Figure 4 Typical transient thermal impedance $Z_{thJA} = f(t_p)$, T_a = 85°C
Value is according to Jedec JESD51-2, at natural convection on FR4 boards. Where applicable a thermal via array under the ex posed pad contacted the first inner copper layer. Device is dissipating 1 W power.

4 Power Stage

4.1 Output On-state Resistance

The on-state resistance depends on the supply voltage (V_{DD}) and on the junction temperature (T_J). **Figure 5** shows these dependencies. The behavior in reverse polarity is described in chapter**"Reverse Current Capability" on Page 15**.

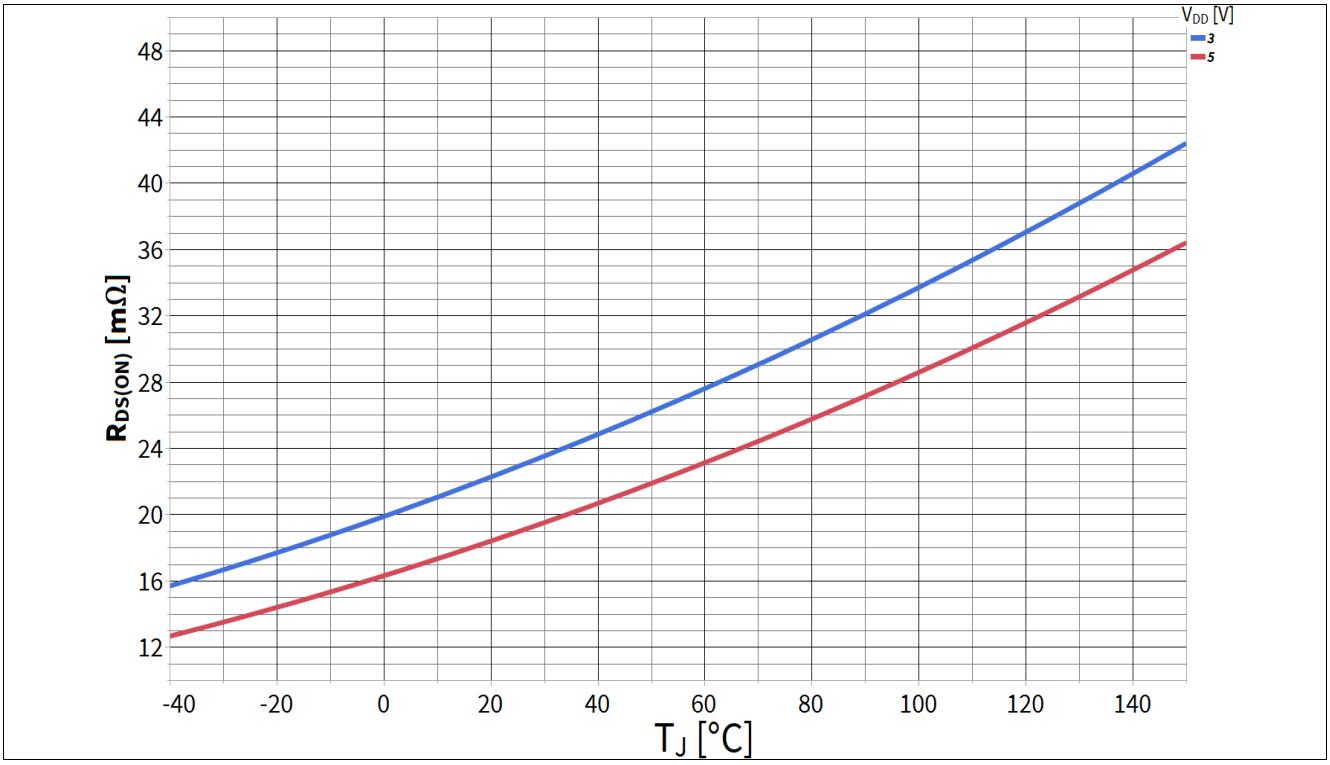


Figure 5 Typical On-State Resistance, $R_{DS(ON)} = f(T_J)$; $V_{DD} = V_{IN} = 5$ V, 3 V

4.2 Resistive Load Output Timing

Figure 6 shows the typical timing when switching a resistive load.

Both $-(\Delta V/\Delta t)_{ON}$ and $(\Delta V/\Delta t)_{OFF}$ can be calculated using the following formulas:

Turn-on Slew rate: $-(\Delta V/\Delta t)_{ON} = (0.6 \times V_{BAT}) / t_F$
Turn-off Slew rate: $(\Delta V/\Delta t)_{OFF} = (0.6 \times V_{BAT}) / t_R$

NB: the coefficient 0.6 is based on 20% to 80% of V_{BAT}, this is how the measurement of ΔV is defined.

As shown in **Figure 6** t_{ON} and t_{OFF} can be calculated from delay time (t_{DON}, t_{DOFF}) and falling/rising time (t_F, t_R) using the following formulas:

Turn-on time: $t_{ON} = t_{DON} + t_F$
Turn-on time: $t_{OFF} = t_{DOFF} + t_R$

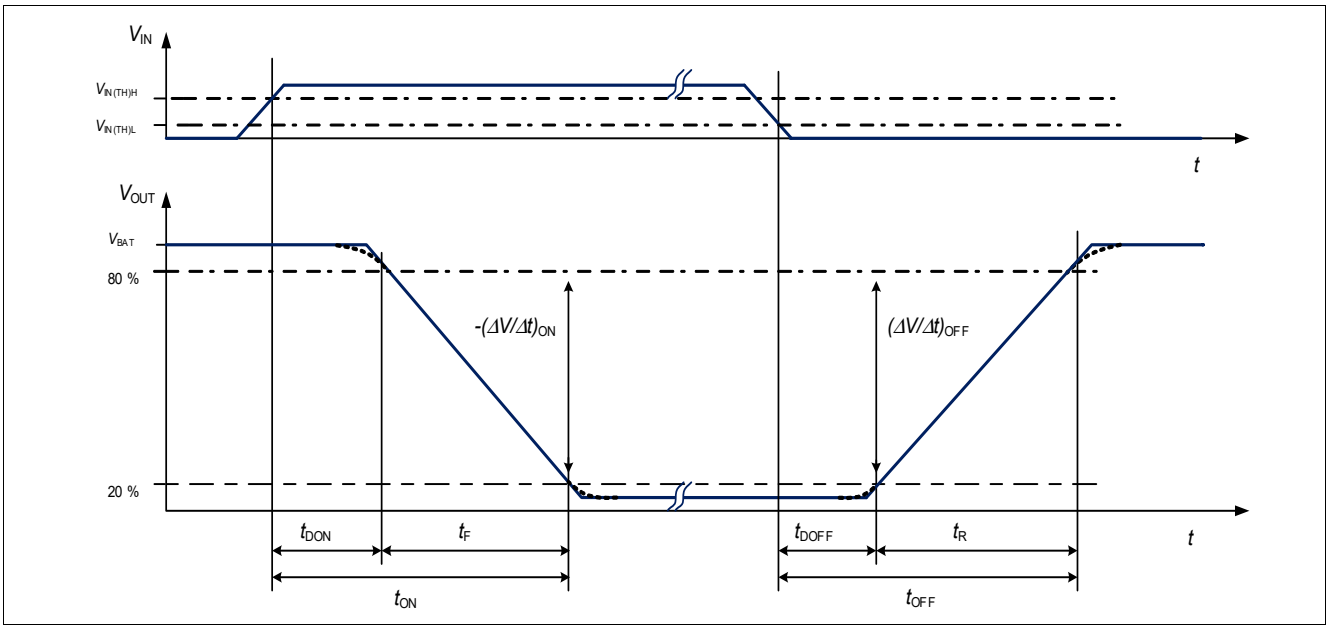


Figure 6 Definition of Power Output Timing for Resistive Load

4.3 Adjustable switching speed / Slew rate

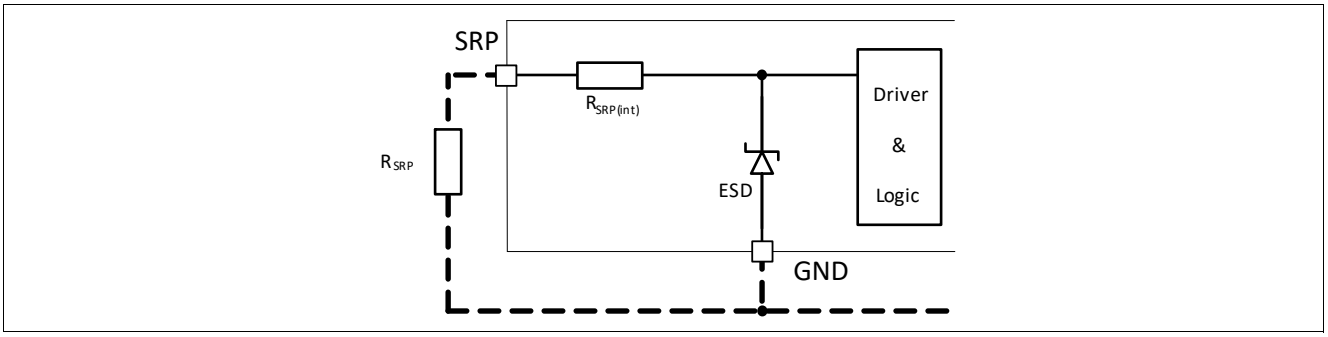


Figure 7 Simplified SRP circuit

Figure 7 shows the slew rate control circuit of the BTT3018EJ. The circuit includes an ESD protection mechanism via a zener structure.

In order to optimize the switching speed of the MOSFET to a specific application, an external resistor can be connected between SRP pin and GND to select the desired slew rate (see switching timings in **Chapter 8.1**). The adjustment of the slew rate also allows to balance between electromagnetic emissions and power dissipation.
To reduce the number of external components, the SRP pin can be connected directly to GND. This sets the slew rate at its largest value enabling fast switching timings.

It is not recommanded to connected directly SRP pin to V_{DD} or to leave it floating (open).
The accuracy of the switching speed is dependent on the accuracy of the external resistor used. It is recommended to use short connections between the SRP pin and either R_{SRP}, GND bias.

Figure 8 show the typical relation between switching speed and the external SRP resistor (R_{SRP}).

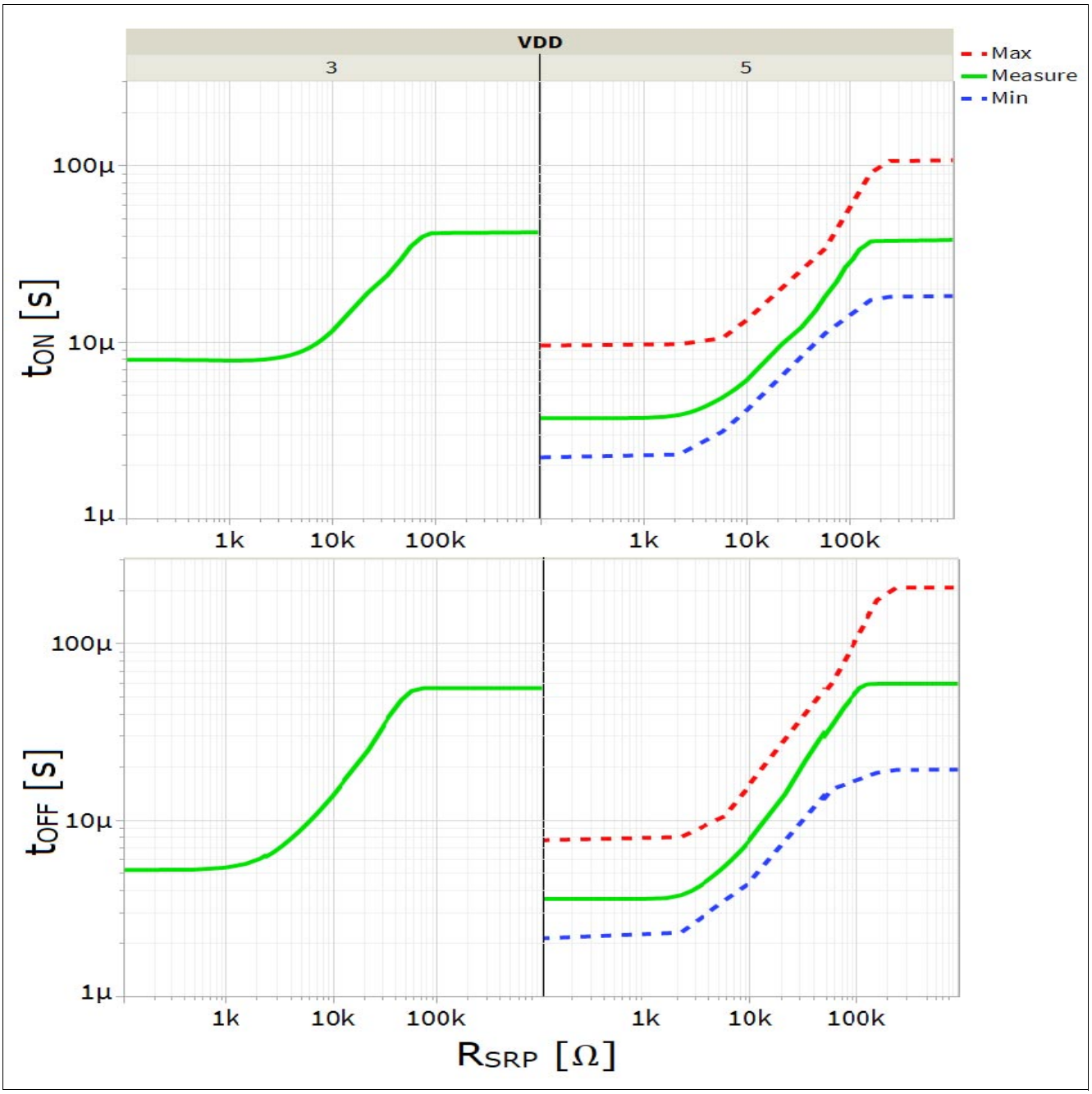


Figure 8 Typical diagram representing the relation between R_{SRP} and t_{ON}, t_{OFF}; V_{DD}= 3V, 5V

4.3.1 Output Clamping

When switching off inductive loads with low side switches, the drain-source voltage V_{OUT} rises above the battery potential due to the inductance tendency to continue driving the current. To prevent unwanted high voltages, the device has a voltage clamping mechanism to keep the voltage at $V_{OUT(CLAMP)}$. During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See **Figure 9** and **Figure 10** for more details.

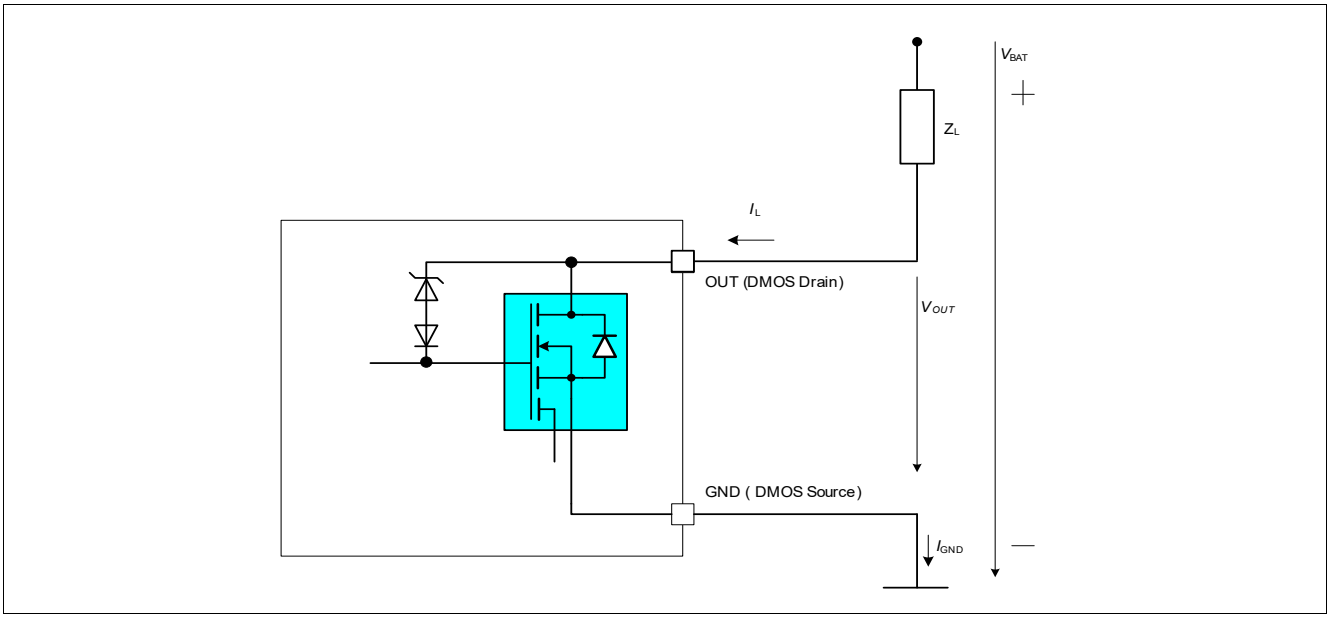


Figure 9 Output Clamp Circuitry

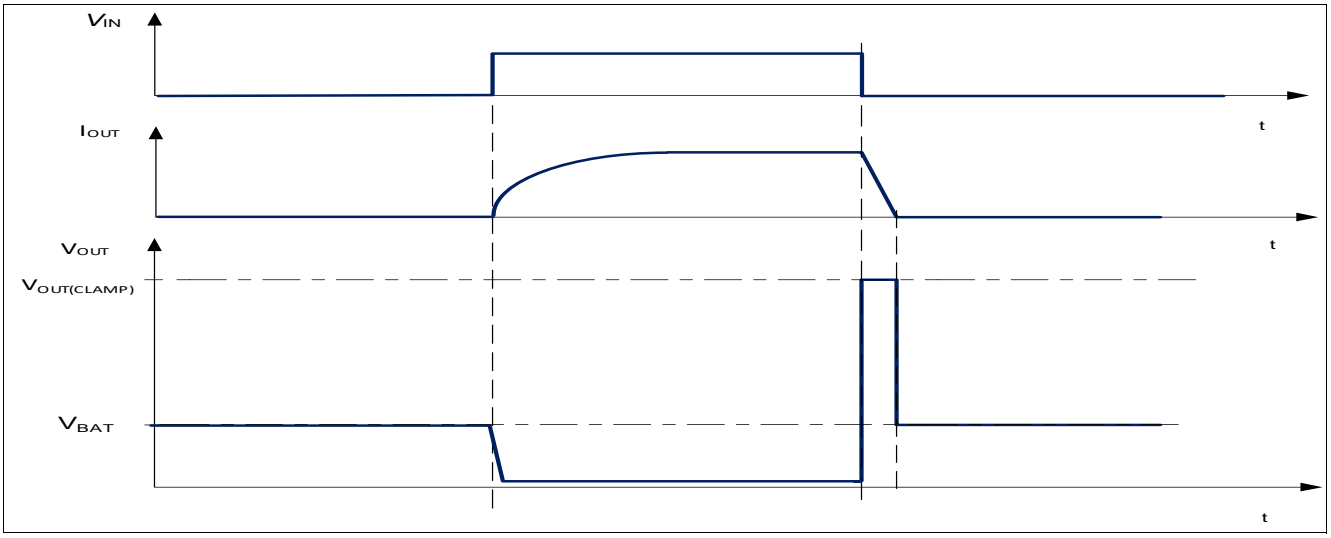


Figure 10 Switching an Inductive Load

Note: Repetitive switching of an inductive load by V_{DD} instead of using the input pin is a not recommended operation and may affect the device reliability and reduce the lifetime.

4.3.2 Maximum Load Inductance

During the demagnetization of inductive loads, energy has to be dissipated by the device.
This energy can be calculated by the following equation:

$$E = V_{OUT(CLAMP)} \times \left[\frac{V_{BAT} - V_{OUT(CLAMP)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_{BAT} - V_{OUT(CLAMP)}}\right) + I_L \right] \times \frac{L}{R_L} \quad (4.1)$$

Following equation is simplified under the assumption of $R_L = 0$

$$E = \frac{1}{2} L I_L^{\,2} \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CLAMP)}}\right) \quad (4.2)$$

Figure 11 shows the inductance for a given current the device BTT3018EJ can withstand.

For maximum single avalanche energy please also refer to E_{AS} parameter in **Chapter 3.1**

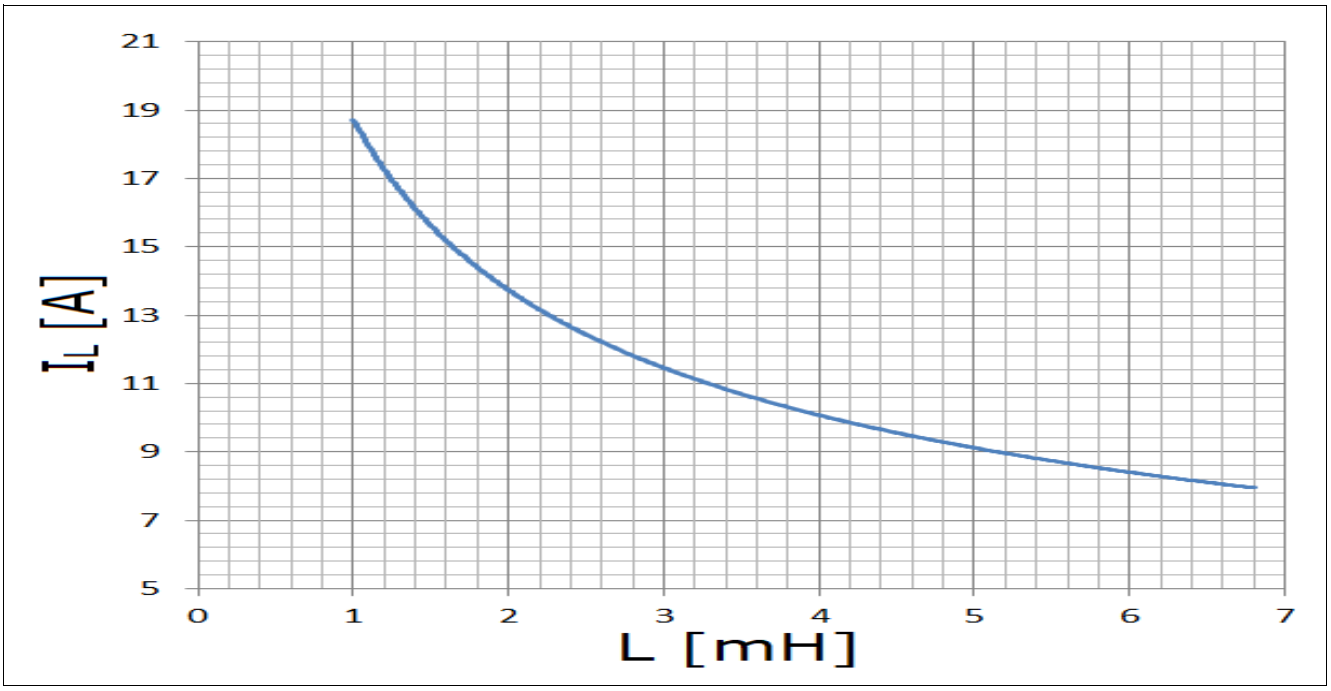


Figure 11 Maximum load inductance for single pulse
$I_L = f(L)$; $T_{J(0)} = 150$ °C; $V_{BAT} = 28$ V

4.4 Reverse Current Capability

A reverse battery situation means that the device drain is pulled below GND potential to $-V_{BAT}$. In this situation the load is driven by a current through the intrinsic body diode of the BTT3018EJ and all protections, such as current limitation, over temperature or over voltage clamping, are not active.

In inverse or reverse operation via the reverse body diode, the device is dissipating a power loss which is defined by the driven current and the voltage drop on the body diode.

4.5 Characteristics

Please see **"Power Stage" on Page 23** for electrical characteristic table.

5 Supply and Input Stage

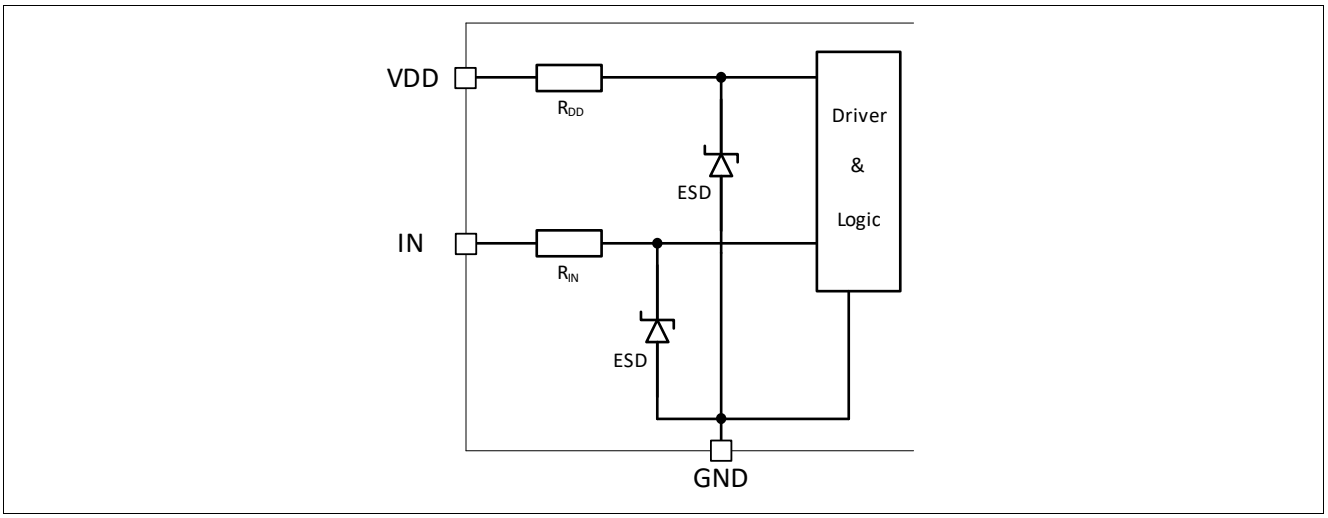


Figure 12 Simplified supply and input circuit

Figure 12 shows the supply and input circuit of the BTT3018EJ. Both terminals include an ESD protection mechanism via a zener structure.

5.1 Supply Circuit

The device's supply is not internally regulated but provided by an external supply. Therefore a reverse polarity protected and buffered (3.3V .. 5.5V) voltage supply is required at V_{DD} pin. To achieve the best $R_{DS(ON)}$ and the fastest switching speed a 5V supply is required.

5.1.1 Undervoltage Shutdown

In order to ensure a stable device behavior under all allowed conditions, the supply voltage V_{DD} is monitored.

The output switches off if the supply voltage V_{DD} drops below the switch-off threshold $V_{DD(TH)L}$. If the supply voltage V_{DD} drops below the supply voltage reset threshold $V_{DD(RESET)}$, a reset of the STATUS signal and the latch-OFF state will occur. The device functions are only given for supply voltages above the supply voltage threshold $V_{DD(TH)H}$.

5.1.2 Supply current consumption

The supply current consumption is determined by the state of the IN pin, being low, with the $I_{DD(OFF)}$ and being high, with the $I_{DD(ON)}$. After a thermal shutdown, when the device is in OFF latch mode, the current consumption values matches the normal ON state $I_{DD(ON)}$ as long as input is high.

However in PWM the consumption depends on the switching frequency. The higher the frequency, the higher the $I_{DD(PWM)}$.

Figure 13 shows the typical relation between the supply current consumption and the switching frequency considering a duty-cycle of 50%.

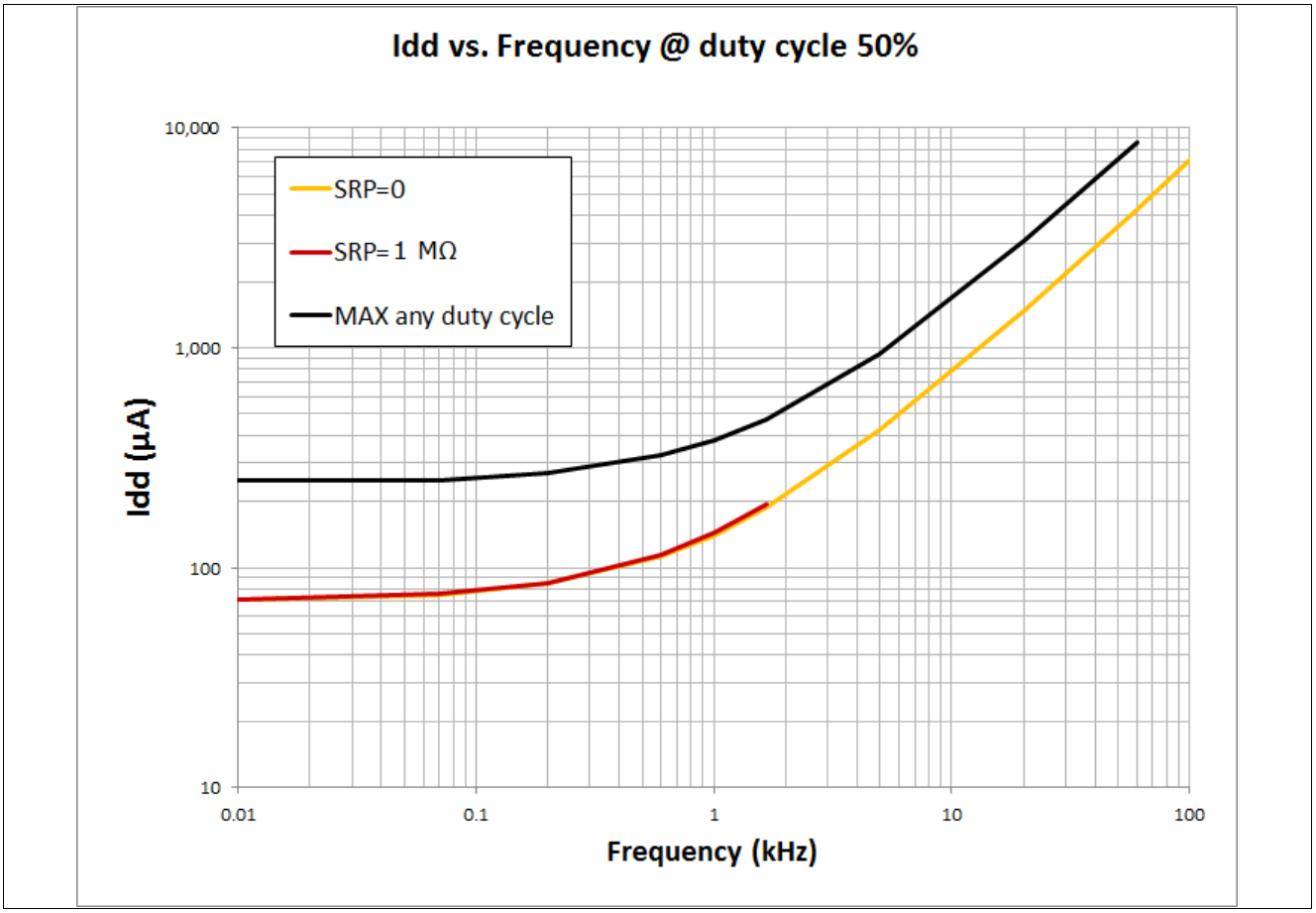


Figure 13 Typical $I_{DD(PWM)}$ vs switching frequency at 50% duty-cycle

5.2 Characteristics

Please see **"Supply and Input Stage" on Page 26** for electrical characteristic table.

6 Protection Functions

The BTT3018EJ provides embedded protection functions. They are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operation. Protection functions are not to be used for continuous or repetitive operation.

6.1 Over Voltage Clamping on Output

The BTT3018EJ is designed with a voltage clamp circuitry that limits the drain-source voltage V_{DS} at a certain level $V_{OUT(CLAMP)}$. The over voltage clamping is overruling the other protection functions. Power dissipation has to be limited to not exceed the maximum allowed junction temperature.

This function is also used in terms of inductive clamping. Please see also **“Output Clamping” on Page 14** for more details.

6.2 Thermal Protection

The device is protected against over temperature due to overload and/or bad cooling conditions by an integrated static temperature sensor. The thermal protection is available when the device is active. In the event of over temperature shutdown $T_{J(SD)}$, the device will remain OFF until the device is reset via STATUS pin. Please see **Figure 14** and **Figure 15**.

6.3 Overcurrent Limitation / Short Circuit Behavior

This BTT3018EJ provides an overcurrent limitation intended to protect against short circuit or over current conditions.

When the drain current reaches the current limitation level $I_{L(LIM)}$, the device will limit the current at that level. While doing so, the power dissipation will heat up the device. Once the device reaches the over temperature shutdown threshold $T_{J(SD)}$, it will automatically shutdown and remain OFF until it is reset via STATUS pin.

6.4 Reset latch condition

The reset of the latch OFF mode is done in two steps that need to be performed in the correct sequence. During the first step, the voltage at the STATUS pin must be below the $V_{STATUS(RESET)L}$ threshold for a time t > $t_{STATUS(RESET)L}$. In the second step of the reset sequence, the STATUS pin voltage needs to be pulled-up above the $V_{STATUS(RESET)H}$ threshold for a time t > $t_{STATUS(RESET)H}$. The total reset time is given by the sum of $t_{STATUS(RESET)L}$ and $t_{STATUS(RESET)H}$.
The following sub-chapters explain in more details the reset functionality in different conditions.

Reset via STATUS pin

If the temperature protection shutdowns the device, it will remain latched OFF independently of the input signal at IN pin. Simultaneously, the STATUS pin signal will be signalized low $V_{STATUS(LATCH)}$. In order to reset the latch condition, the STATUS pin needs to remain below $V_{STATUS(RESET)L}$ for a minimum time $t_{STATUS(RESET)L}$ before being externally pulled-up to $V_{STATUS(RESET)H}$ for a minimum time $t_{STATUS(RESET)H}$. Please refer to **Figure 14** and the application diagram in **Figure 33**.
This configuration allows the device to be driven with high frequency PWM signal via the IN pin without a risk of resetting the device in case it goes in protection shut-down mode (latch OFF).

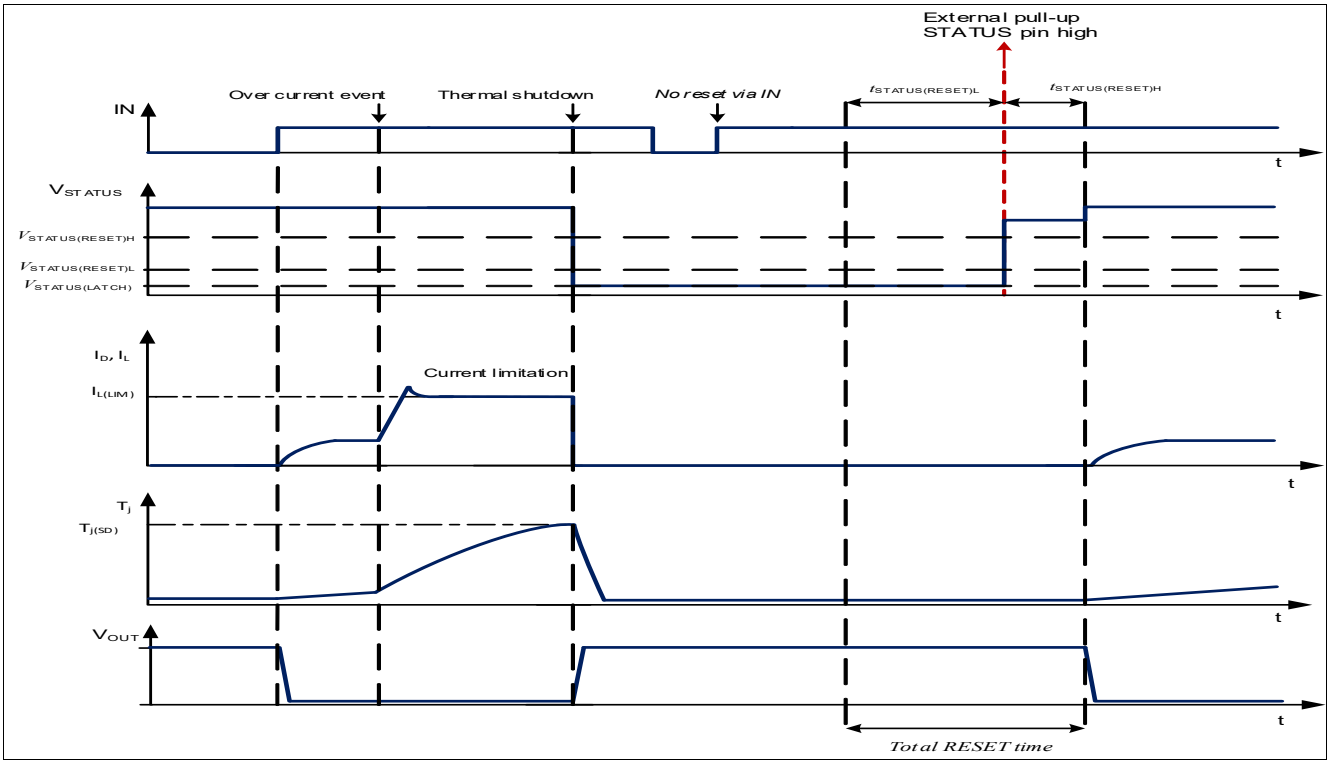


Figure 14 Mechanism to reset latch condition via STATUS pin

Reset via STATUS pin and IN pin connected together

If STATUS pin and IN pin are connected together (No R_{STATUS} pull-up external resistor), the voltage provided through the IN pin will prevent the STATUS low notification. To reset the device under this condition, the STATUS-IN connection needs to be pulled-down to $V_{STATUS(RESET)L}$ for a minimum time $t_{STATUS(RESET)L}$ before being pulled-up to $V_{STATUS(RESET)H}$ for a minimum time $t_{STATUS(RESET)H}$. Please refer to **Figure 15** and the application diagram in **Figure 34**.

If no diagnosis of the device is required, this configuration avoids the need of a dedicated I/O from the microcontroller for the STATUS pin. The maximum frequency to not reset the device allowed in PWM mode is constrained by the $t_{STATUS(RESET)L}$ and $t_{STATUS(RESET)H}$ times.

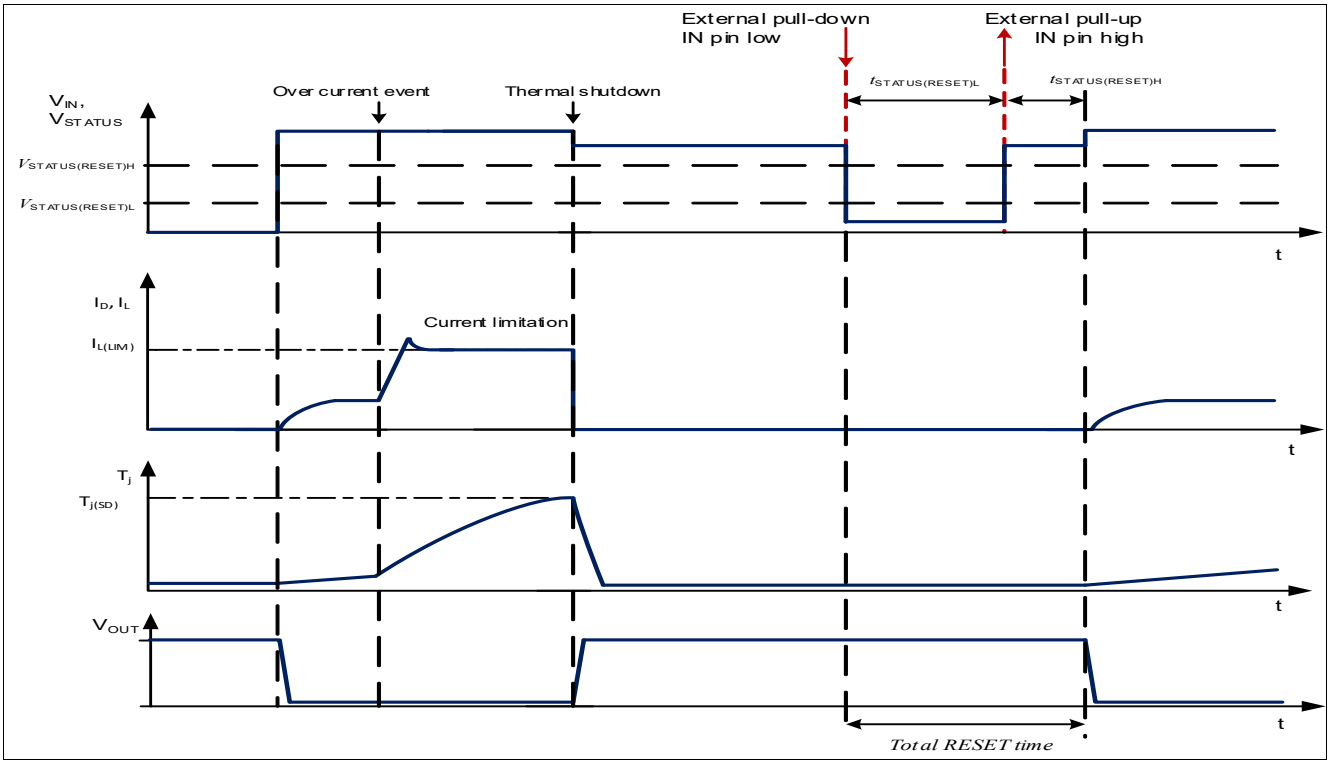


Figure 15 Mechanism to reset latch condition with STATUS pin and IN pin connected together

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

6.5 Characteristics

Please see **"Protection" on Page 25** for electrical characteristic table.

7 Diagnostics

The BTT3018EJ provides a latching digital fault feedback signal on the STATUS pin triggered by an over temperature shutdown.

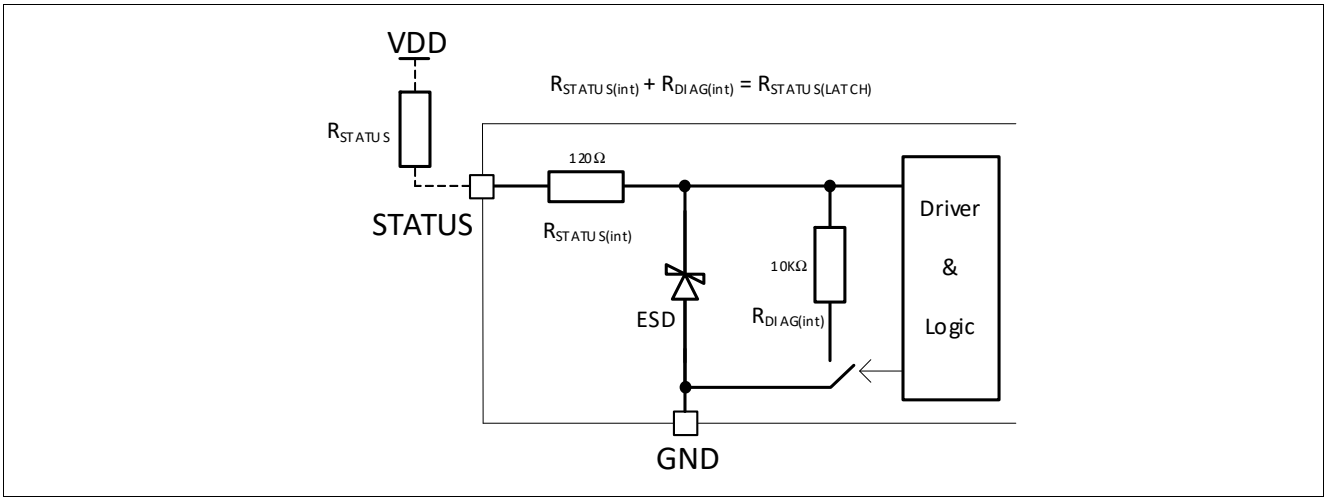


Figure 16 Simplified diagnosis circuit

Figure 16 shows the diagnosis circuit of the BTT3018EJ. The circuit include an ESD protection mechanism via a zener structure. Note that $R_{STATUS(int)} + R_{DIAG(int)} = R_{STATUS(LATCH)}$ (cf. P_8.5.12).

7.1 Functional Description of the STATUS Pin

The BTT3018EJ provides digital status information via the STATUS pin to give feedback to a connected microcontroller.

The readout of the diagnosis signal is only possible if the STATUS pin has a dedicated connection to the microcontroller and the appropriate pull-up resistor R_{STATUS} is in place. See **Figure 33** for recommended values of the external components.

The device is able to operate with STATUS pin and IN pin connected together, however this condition will inhibit the readout of the diagnosis signal.

Normal operation mode

In normal operation (no thermal shutdown) the STATUS pin's logic is set "high". It is pulled-up via an external Resistor (R_{STATUS}) to V_{DD}. Internally it is connected to an open drain MOSFET through an internal resistor.

Fault operation mode

In case of a thermal shutdown (fault) the internal MOSFET connected to the STATUS pin, pulls it's voltage down to GND providing a "low" level signal to the microcontroller $V_{STATUS(LATCH)}$. Fault mode operation remains active independent from the input pin state until it is reset.

Reset latch fault signal (external pull up)

To reset the latch fault signal of the BTT3018EJ, the STATUS pin has to be externally pulled-up. This behavior is shown in **Figure 14 "Mechanism to reset latch condition via STATUS pin" on Page 19**.

For other configurations and how to reset the latch OFF of the DMOS, please see **"Reset latch condition" on Page 18**.

7.2 Characteristics

Please see **“Diagnostics” on Page 28** for electrical characteristic table.

8 Electrical Characteristics

Note: Characteristics show the deviation of parameter at given input voltage and junction temperature. Typical values show the typical parameters expected from manufacturing and in typical application condition.
All voltages and currents naming and polarity in accordance to ***Figure 2.3 "Voltage and Current Definition" on Page 7****.*

8.1 Power Stage

Please see Chapter **"Power Stage" on Page 11** for parameter description and further details.

Table 5 Electrical Characteristics: Power Stage

T_j = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Stage - Static Characteristics							
On-State resistance at 5 V supply and 25°C	$R_{DS(ON)\_5\_25}$	–	16	20	mΩ	V_{DD} = 5 V; T_J = 25°C	P_8.1.1
On-State resistance at 5 V supply and 150°C	$R_{DS(ON)\_5\_150}$	–	33	38	mΩ	V_{DD} = 5 V; T_J = 150°C	P_8.1.2
On-State resistance at 3 V supply and 25°C	$R_{DS(ON)\_3\_25}$	–	20	30	mΩ	V_{DD} = 3 V; T_J = 25°C	P_8.1.3
On-State resistance at 3 V supply and 150°C	$R_{DS(ON)\_3\_150}$	–	39	50	mΩ	V_{DD} = 3 V; T_j = 150°C	P_8.1.4
Nominal load current	$I_{L(NOM)}$	–	7.0	–	A	1) T_J < 150°C; T_A = 85°C; V_{DD} = 5 V;	P_8.1.5
OFF state load current, Output leakage current	$I_{L(OFF)\_85}$	–	0	3.0	µA	2) $T_J \leq$ 85°C $V_{BAT(NOR)}$	P_8.1.6
OFF state load current, Output leakage current at 150°C	$I_{L(OFF)\_150}$	–	4	30	µA	T_J = 150°C $V_{BAT(NOR)}$	P_8.1.7
Body Diode							
Reverse diode forward voltage	$-V_{DS}$	–	0.6	1	V	V_{IN} = 0 V	P_8.1.8
Switching times. R_{SRP} = short to GND; V_{BAT} = 28 V; V_{DD} = 5 V; R_{Load} = 4.7 Ω see Figure 6 for definition details							
Turn-on delay time	$t_{DON\_5(0)}$	1.6	2.7	6.8	µs	-	P_8.1.11
Turn-off delay time	$t_{DOFF\_5(0)}$	1.5	2.8	5.5	µs	-	P_8.1.12
Turn-on output fall time	$t_{F\_5(0)}$	0.5	1.4	2.5	µs	-	P_8.1.13

Table 5 Electrical Characteristics: Power Stage (cont'd)

T_j = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Turn-off output rise time	$t_{R\_5(0)}$	0.3	0.8	1.7	µs	-	P_8.1.14
Switching times. R_{SRP} = 5.8 KΩ;V_{BAT} = 28 V; V_{DD} = 5 V; R_{Load} = 4.7 Ω see Figure 6 for definition details							
Turn-on delay time	$t_{DON\_5(5K8)}$	2.0	3.1	6.9	µs	-	P_8.1.33
Turn-off delay time	$t_{DOFF\_5(5K8)}$	2.4	4.5	7.6	µs	-	P_8.1.34
Turn-on output fall time	$t_{F\_5(5K8)}$	1.1	2.1	3.6	µs	-	P_8.1.35
Turn-off output rise time	$t_{R\_5(5K8)}$	1.0	1.7	2.9	µs	-	P_8.1.36
Switching times. R_{SRP} = 58 KΩ;V_{BAT} = 28 V; V_{DD} = 5 V; R_{Load} = 4.7 Ω see Figure 6 for definition details							
Turn-on delay time	$t_{DON\_5(58K)}$	5.5	10.5	15.3	µs		P_8.1.55
Turn-off delay time	$t_{DOFF\_5(58K)}$	8	20.4	40.9	µs		P_8.1.56
Turn-on output fall time	$t_{F\_5(58K)}$	5.7	11.3	18.6	µs		P_8.1.57
Turn-off output rise time	$t_{R\_5(58K)}$	6.9	12.8	19.3	µs		P_8.1.58
Switching times. R_{SRP} = 1 MΩ;V_{BAT} = 28 V; V_{DD} = 5 V; R_{Load} = 4.7 Ω see Figure 6 for definition details							
Turn-on delay time	$t_{DON\_5(1M)}$	9.3	17.0	42.2	µs	-	P_8.1.77
Turn-off delay time	$t_{DOFF\_5(1M)}$	10.4	44.2	139	µs	-	P_8.1.78
Turn-on output fall time	$t_{F\_5(1M)}$	8.9	26.7	64.7	µs	-	P_8.1.79
Turn-off output rise time	$t_{R\_5(1M)}$	8.9	27.1	68.2	µs	-	P_8.1.80

1) Not subject to production test, calculated by R_{thJA} and $R_{DS(ON)}$.

2) Not subject to production test, specified by design

8.2 Protection

Please see Chapter **"Protection Functions" on Page 18** for parameter description and further details.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation

Table 6 Electrical characteristics: Protection

T_j = -40°C to +150°C, V_{BAT} = 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal shutdown							
Static thermal shutdown junction temperature	$T_{J(SD)}$	150	175	200	°C	1)	P_8.2.1
Overtemperature shutdown STATUS delay at 5 V	$t_{TJ(SD)5}$	–	4.5		µs	1) Delay time to trigger STATUS signal V_{DD} = 5 V T_{AMB}=25°C	P_8.2.4
Overtemperature shutdown STATUS delay at 3 V	$t_{TJ(SD)3}$	–	4.2		µs	1) Delay time to trigger STATUS signal V_{DD} = 3 V T_{AMB} = 25°C	P_8.2.7
Overvoltage Protection / Clamping							
Drain clamp voltage	$V_{OUT(CLAMP)}$	63	72	83	V	I_D > 50 mA	P_8.2.8
Current limitation							
Current limitation level	$I_{L(LIM)\_5}$	30	45	60	A	2) V_{DD} = 5 V;	P_8.2.9

1) Not subject to production test, specified by design.

2) Parameter tested at V_{BAT} = 5 V; specified up to V_{BAT} = 36 V.

8.3 Supply and Input Stage

Please see Chapter **“Supply and Input Stage” on Page 16** for description and further details.

Table 7 Electrical Characteristics: Supply and Input

T_j = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply							
Supply on threshold voltage high	$V_{DD(TH)H}$	2.4	2.8	3.0	V		P_8.3.2
Supply off threshold voltage low	$V_{DD(TH)L}$	2.3	2.7	2.9	V	1) DMOS switches OFF below threshold	P_8.3.3
Supply current, continuous ON operation	$I_{DD(ON)}$	–	150	250	µA	ON-state ; V_{IN} = 5V; $I_{L(0)} = I_{L(NOM)}$	P_8.3.5
Standby supply current	$I_{DD(OFF)}$	–	0.3	3	µA	V_{IN} = 0 V V_{DD} = 5.0 V	P_8.3.11

Table 7 Electrical Characteristics: Supply and Input (cont'd)

T_j = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input							
Input on threshold voltage; 5.5 V supply	$V_{IN(TH)H\_5.5}$	1.9	2.4	2.8	V	V_{DD} = 5.5 V	P_8.3.13
Input off threshold voltage; 5.5 V supply	$V_{IN(TH)L\_5.5}$	1.2	1.5	1.8	V	V_{DD} = 5.5 V	P_8.3.14
Input on threshold voltage; 3 V supply	$V_{IN(TH)H\_3}$	1.2	1.5	1.8	V	V_{DD} = 3.0 V	P_8.3.19
Input off threshold voltage; 3 V supply	$V_{IN(TH)L\_3}$	0.7	1.0	1.2	V	V_{DD} = 3.0 V	P_8.3.20
Input pull down current	I_{IN}	20	45	80	µA	$V_{IN} \leq$ 5.5 V; $V_{DD} \leq$ 5.5 V	P_8.3.22

1) Undervoltage shutdown protection doesn't reset the OFF Latch mode.

8.4 Diagnostics

Please see Chapter **"Diagnostics" on Page 21** for description and further details.

Table 8 Electrical Characteristics: Diagnostics

T_j = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Diagnostics							
Status pin latch voltage	$V_{STATUS(LATCH)}$	–	–	1.0	V	1) 2) V_{DD} = 5 V; R_{STATUS} = 100 kOhm; 3 V ≤ V_{IN} ≤ 5 V; latched fault signal	P_8.5.1
Status pin reset threshold low	$V_{STATUS(RESET)L\_5}$	1.0	1.4	1.7	V	3) V_{DD} = 5 V	P_8.5.2
Status pin reset threshold high	$V_{STATUS(RESET)H\_5}$	1.7	2.2	2.6	V	4) V_{DD} = 5 V	P_8.5.3
Status reset low time	$t_{STATUS(RESET)L\_5}$	1.0	1.6	2.4	ms	1)5) V_{DD} = 5 V	P_8.5.4
Status reset high time	$t_{STATUS(RESET)H\_5}$	20	35	50	µs	1)6) V_{DD} = 5 V	P_8.5.5
Status pin reset threshold low	$V_{STATUS(RESET)L\_3}$	0.7	1.0	1.2	V	3) V_{DD} = 3 V	P_8.5.6
Status pin reset threshold high	$V_{STATUS(RESET)H\_3}$	1.2	1.6	1.9	V	4) V_{DD} = 3 V	P_8.5.7
Status reset low time	$t_{STATUS(RESET)L\_3}$	0.5	1.0	2.3	ms	1)5) V_{DD} = 3 V	P_8.5.8
Status reset high time	$t_{STATUS(RESET)H\_3}$	8	15	50	µs	1)6) V_{DD} = 3 V	P_8.5.9
Status pin leakage current; (No Latch)	$I_{STATUS(NOLATCH)}$	–	–	1	µA	1) 3 V ≤ V_{DD} ≤ 5.5 V V_{STATUS} ≤ 5.5 V; 0 V ≤ V_{IN} ≤ 5.5 V	P_8.5.10
Status pin internal resistance, (Latch active)	$R_{STATUS(LATCH)}$	7	10	15	KΩ	$R_{STATUS(LATCH)}$ = $R_{STATUS(int)}$ + $R_{DIAG(int)}$	P_8.5.12

1) Not subject to production test. Specified by design.
2) Latch feedback signal voltage drop considering V_{DD} = 5 V and R_{STATUS} = 100 kOhm.
3) Voltage threshold needed at the STATUS pin to initialize the reset sequence of the latch OFF mode. If STATUS pin and IN pin are connected together, same voltage threshold applies.
4) Voltage threshold needed at the STATUS pin to complete the reset sequence of the latch OFF mode. If STATUS pin and IN pin are connected together, same voltage range applies.
5) Time needed to remain below $V_{STATUS(RESET)L}$ to initialize the reset sequence of the latch OFF mode. See **Chapter 6.4** for more information

6) Time needed to remain above $V_{STATUS(RESET)H}$ after $V_{STATUS(RESET)L}$ is applied to conlude the reset sequence. See **Chapter 6.4** for more information

9 Characterisation Results

Typical performance characteristics

9.1 Power Stage

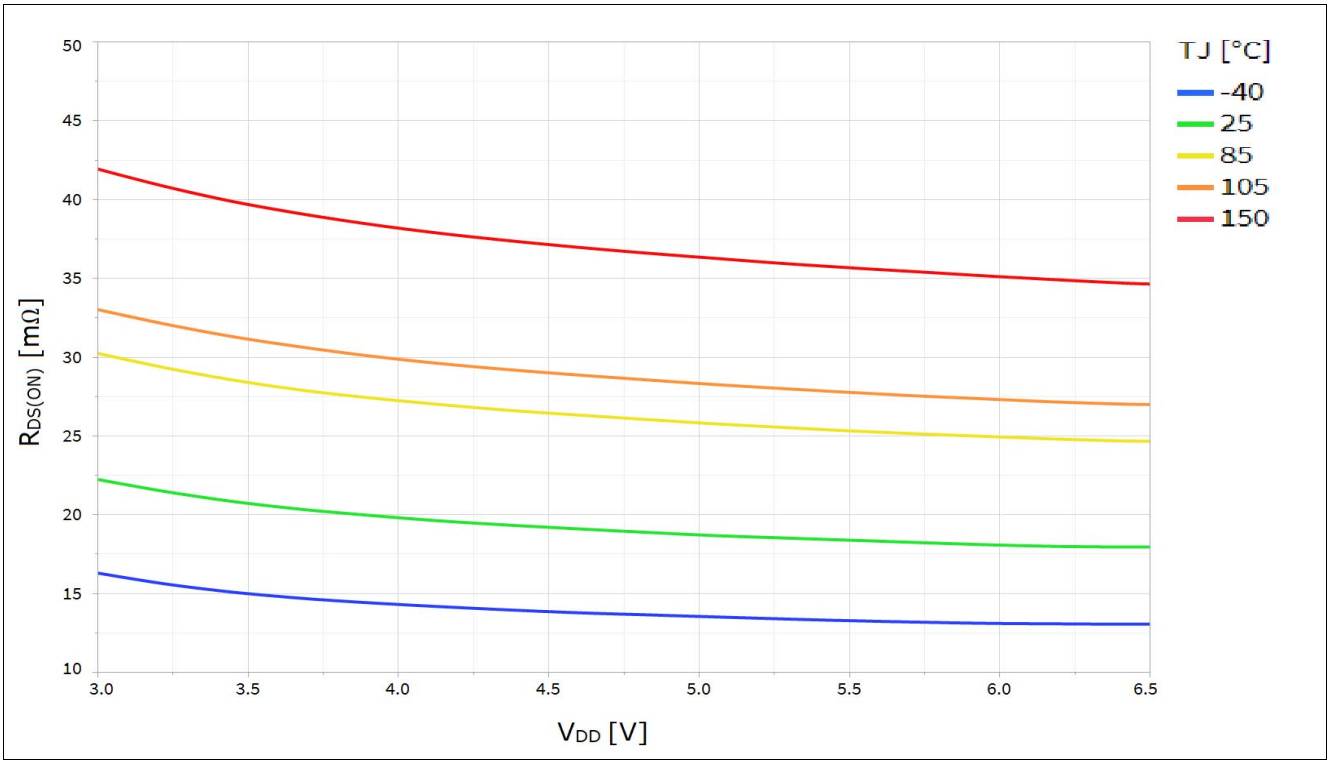


Figure 17 Typical $R_{DS(ON)}$ vs. V_{DD}; I_L=$I_{L(NOM)}$; V_{IN}= 3V; V_{BAT}=28V; R_{SRP}= 0Ω

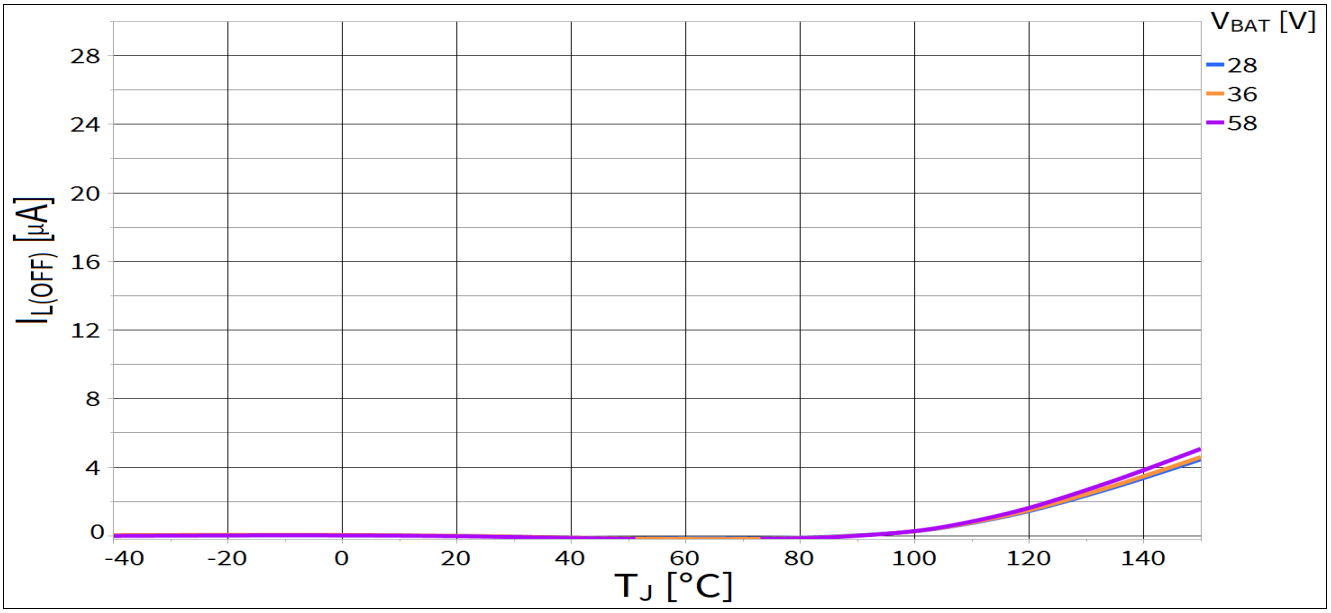


Figure 18 Typical $I_{L(OFF)}$ vs. T_J @ V_{IN} = 0V; V_{DD}= 0, 5V

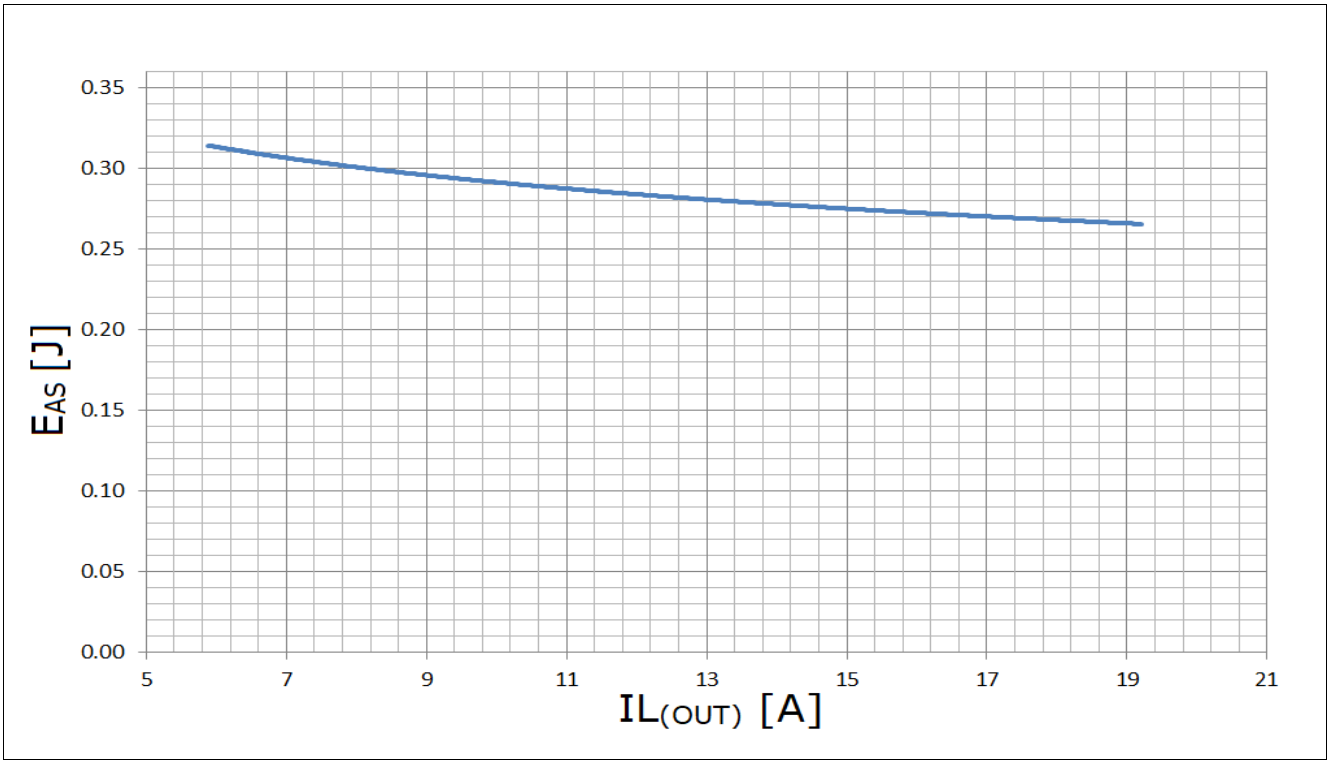


Figure 19 Typical destruction point E_{AS} vs. I_L @ $T_{J(0)}$=150°C; V_{BAT}=28V; I_L= $I_{L(NOM)}$, 2*$I_{L(NOM)}$

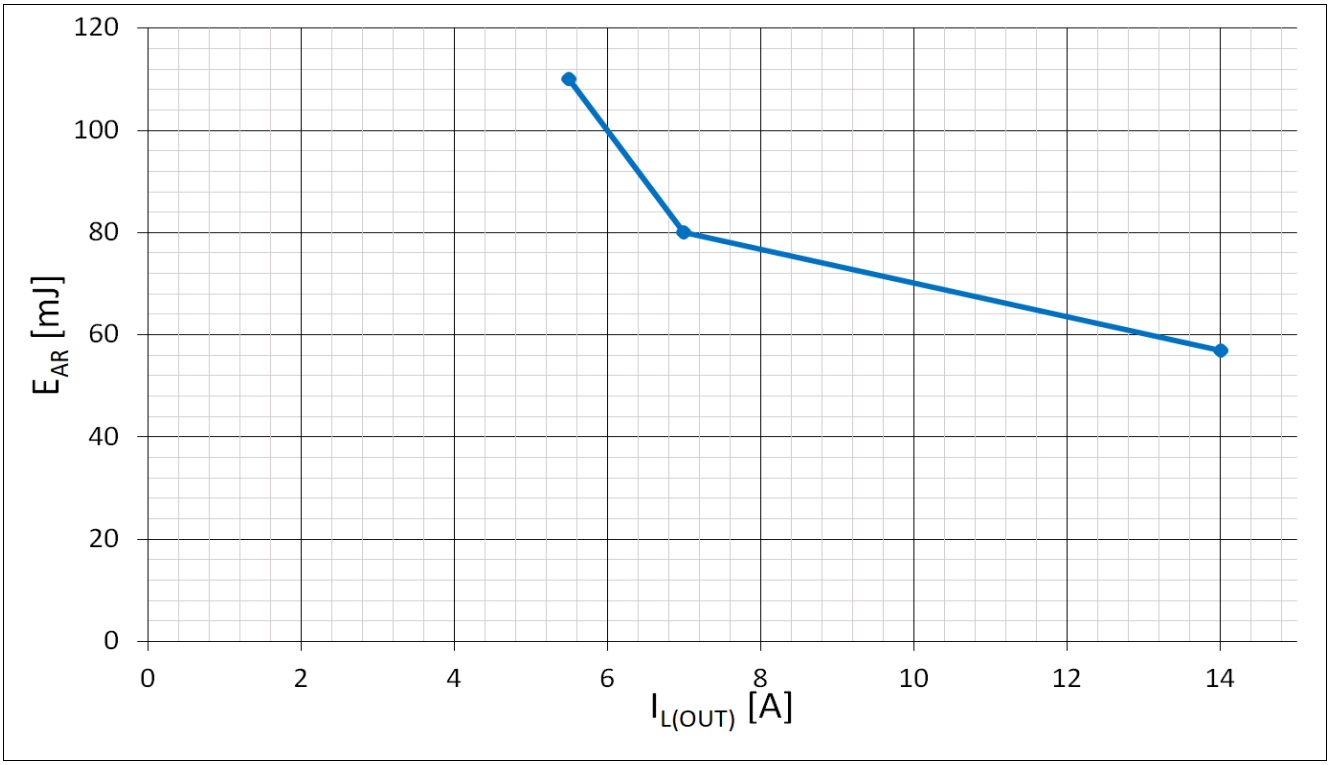


Figure 20 Typical E_{AR} vs. I_L @ $T_{J(0)}$=105°C, V_{BAT}= 28V; Nr cycles = 10k, 100k, 1Mio cycles; I_L = $I_{L(NOM)}$, 2*$I_{L(NOM)}$

Characterisation Results

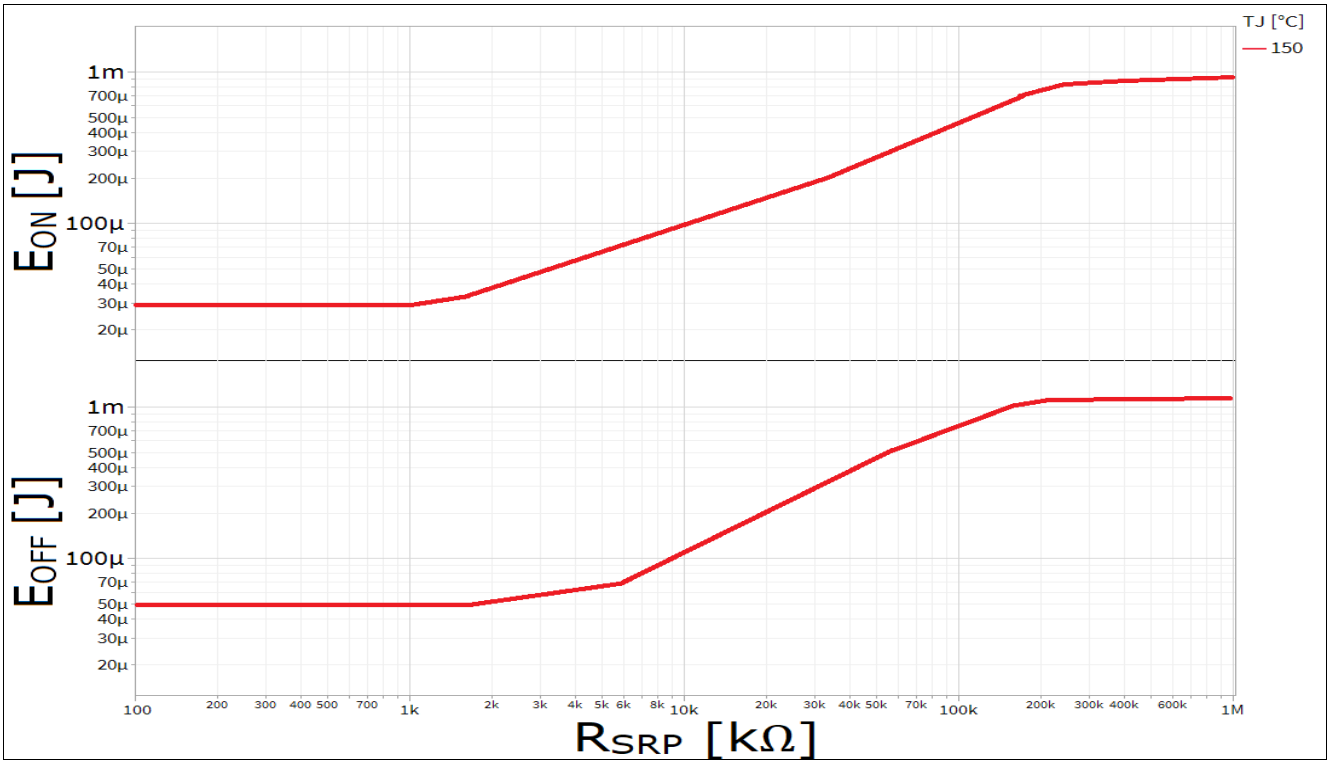


Figure 21 *Typical EON & EOFF vs. SRP @ $T_{J(0)}$=150°C, V_{DD}=5.5V & V_{DD}=3V; V_{BAT}= 28V; IN= 5V; STATUS= pulled-up to V_{DD};* $I_L = I_{L(NOM)}$

Dynamic characteristics

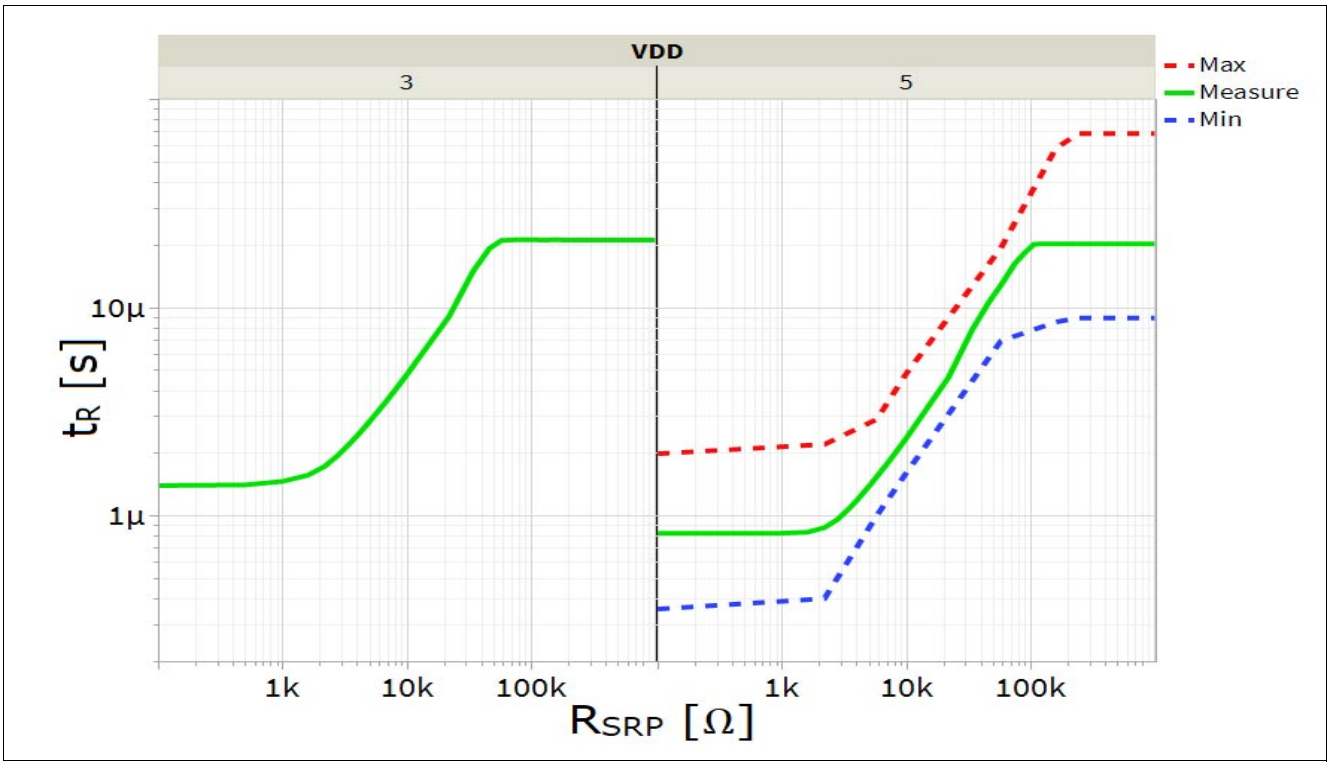


Figure 22 *Typical t_R vs. R_{SRP} @ V_{IN} = 5V; V_{DD}= 3V, 5V; V_{BAT}= 28V; R_L=4.7Ω; T_J=[-40 .. 150°C]*

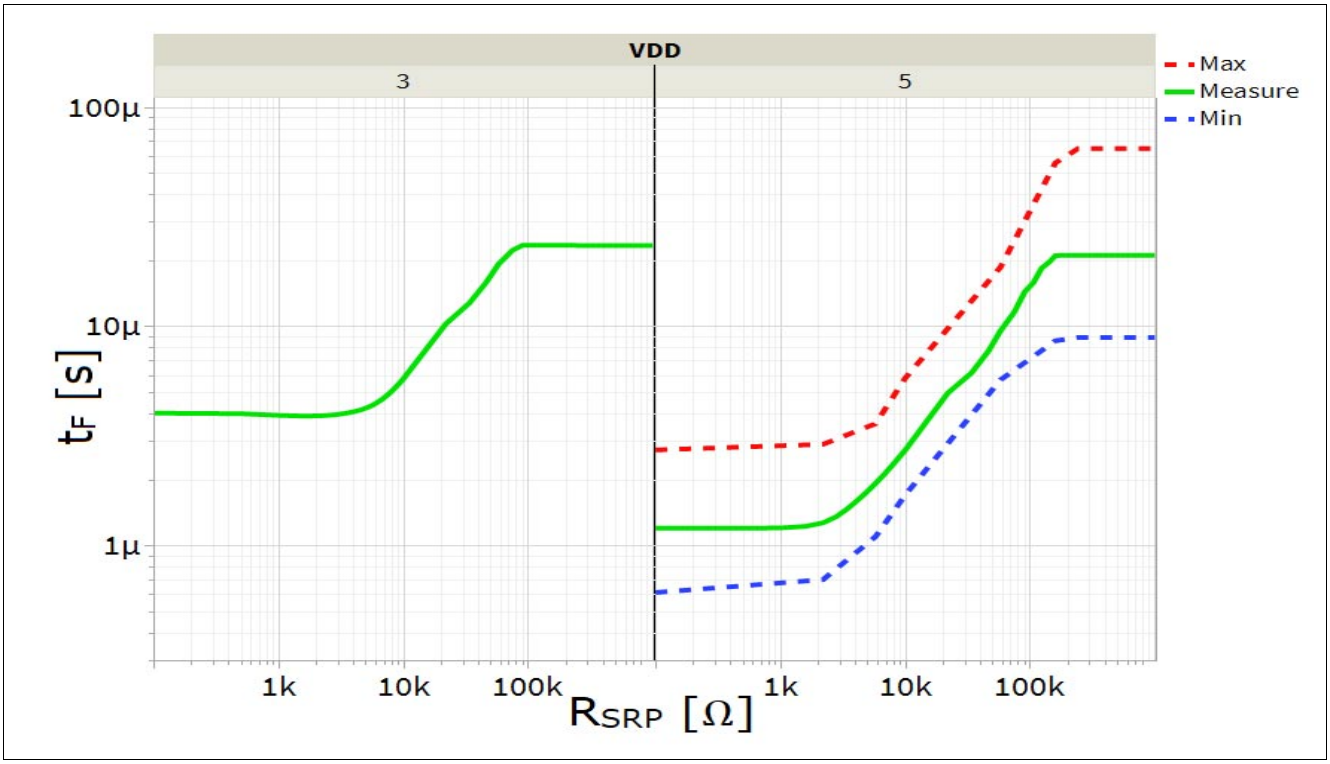


Figure 23 *Typical* t_F **vs.** R_{SRP} **@** V_{IN} **= 5V;** V_{DD}**= 3V, 5V;** V_{BAT}**= 28V;** R_L**=4.7Ω;** T_J**=[-40 .. 150°C]**

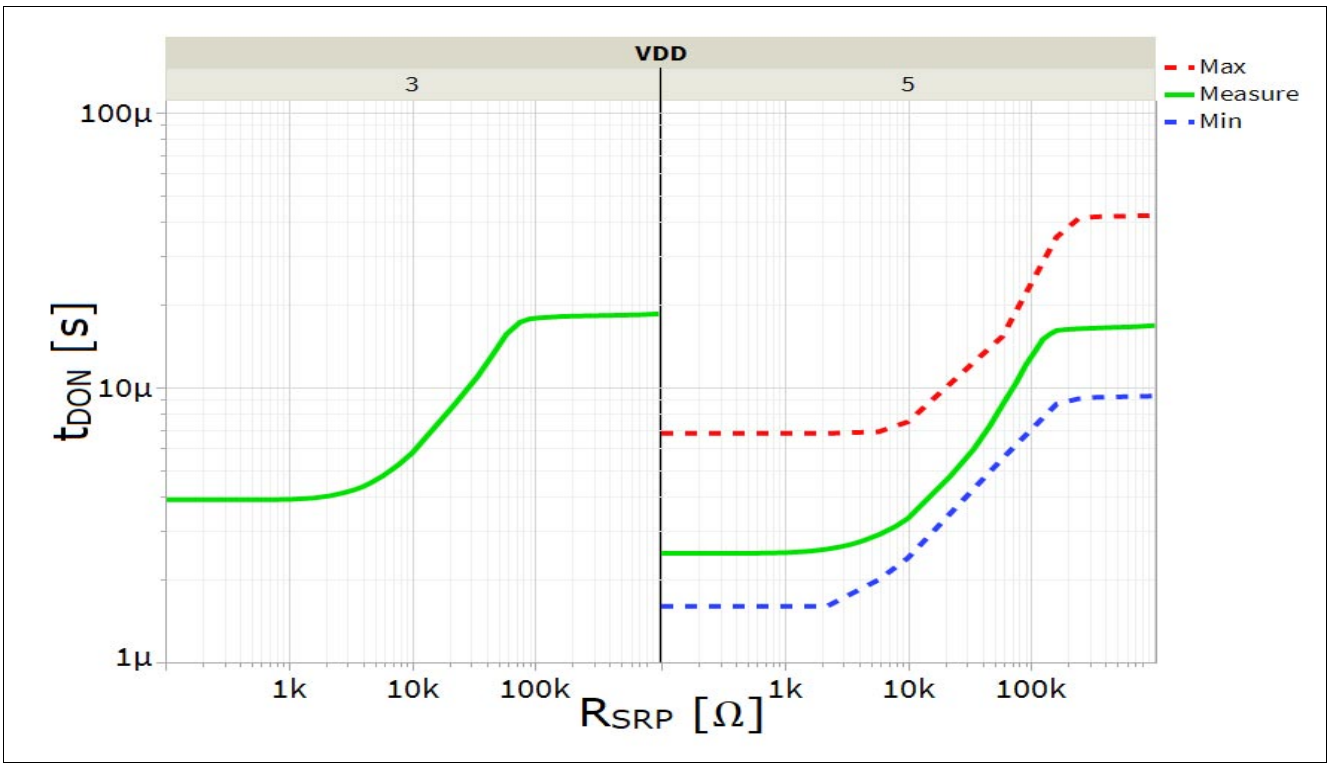


Figure 24 *Typical* t_{DON} **vs.** R_{SRP} **@** V_{IN} **= 5V;** V_{DD}**= 3V, 5V;** V_{BAT}**= 28V;** R_L**=4.7Ω;** T_J**=[-40 .. 150°C]**

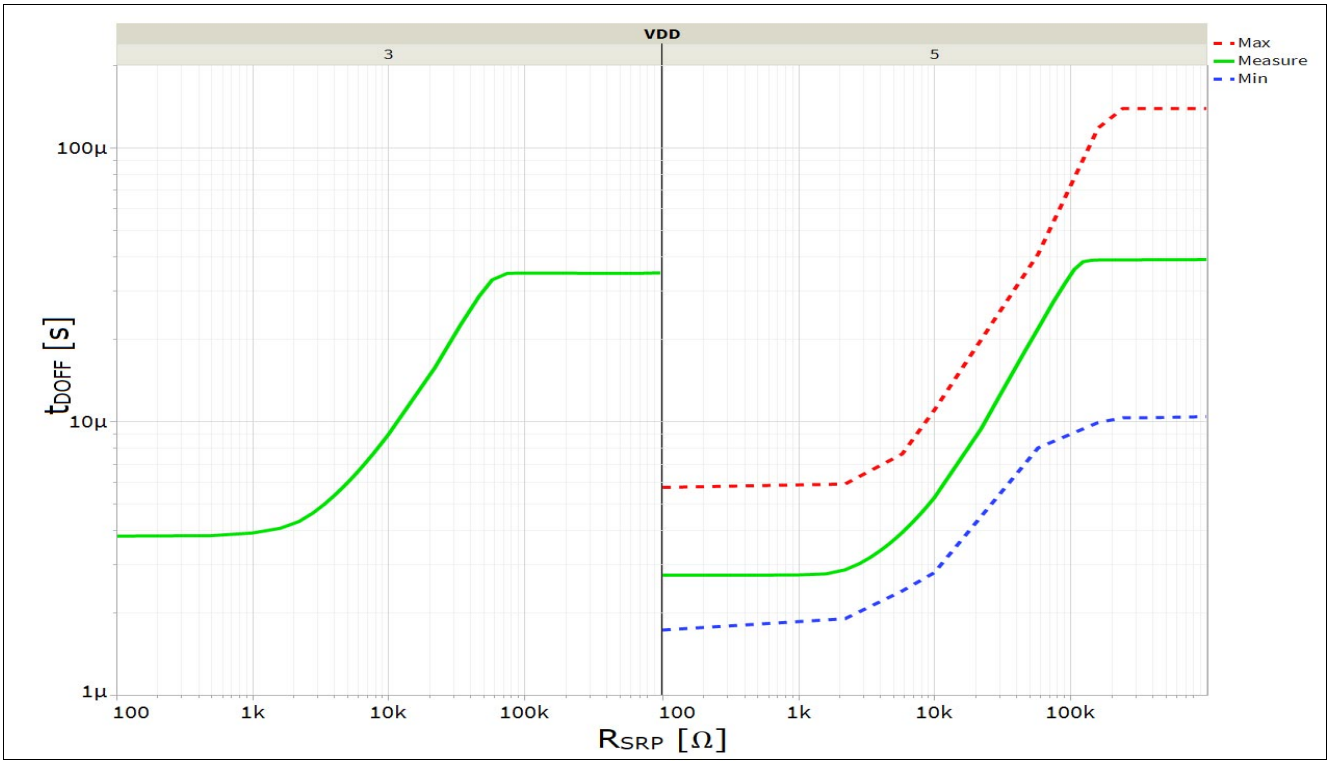


Figure 25 *Typical* t_{DOFF} **vs.** R_{SRP} **@** V_{IN} **= 5V;** V_{DD}**= 3V, 5V;** V_{BAT}**= 28V;** R_L**=4.7Ω;** T_J**=[-40 .. 150°C]**

9.2 Protection

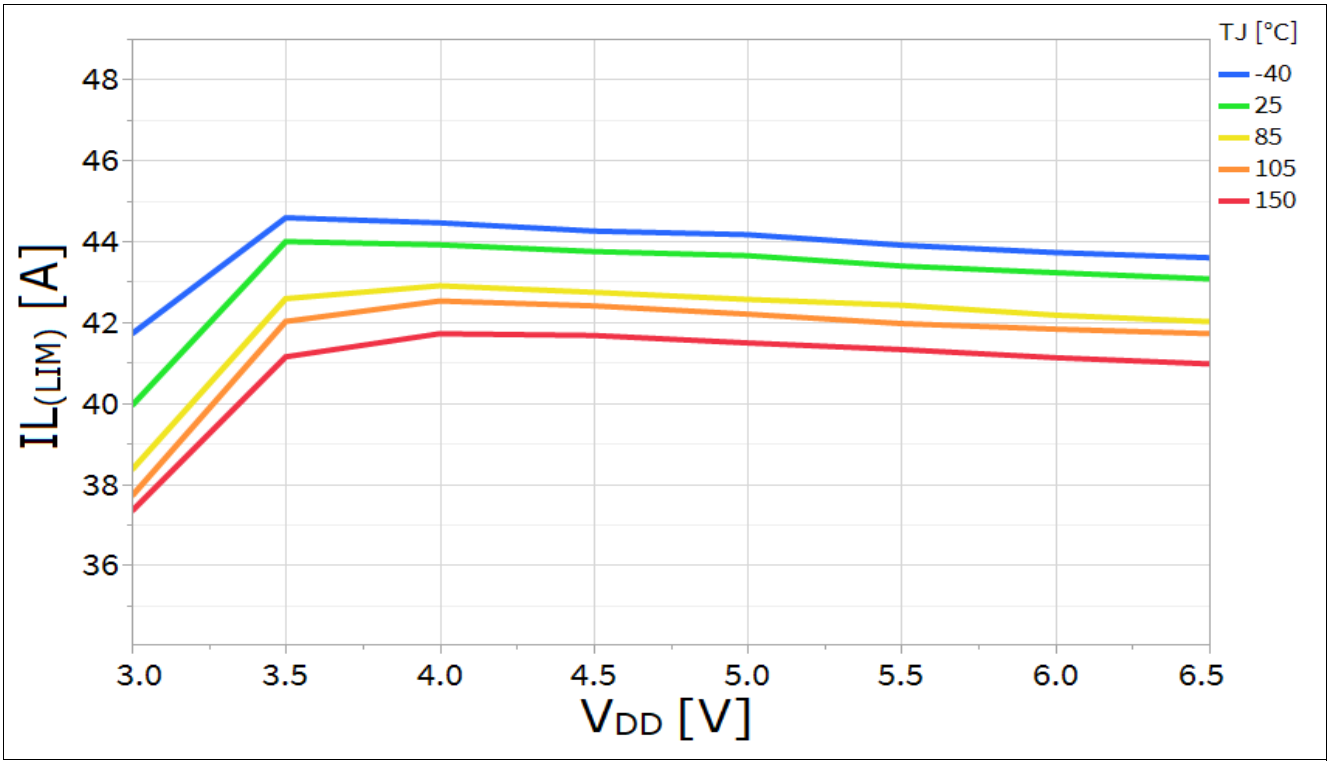


Figure 26 **Typical** $I_{L(LIM)}$ **vs.** V_{DD}**;** V_{IN}**= 5V**

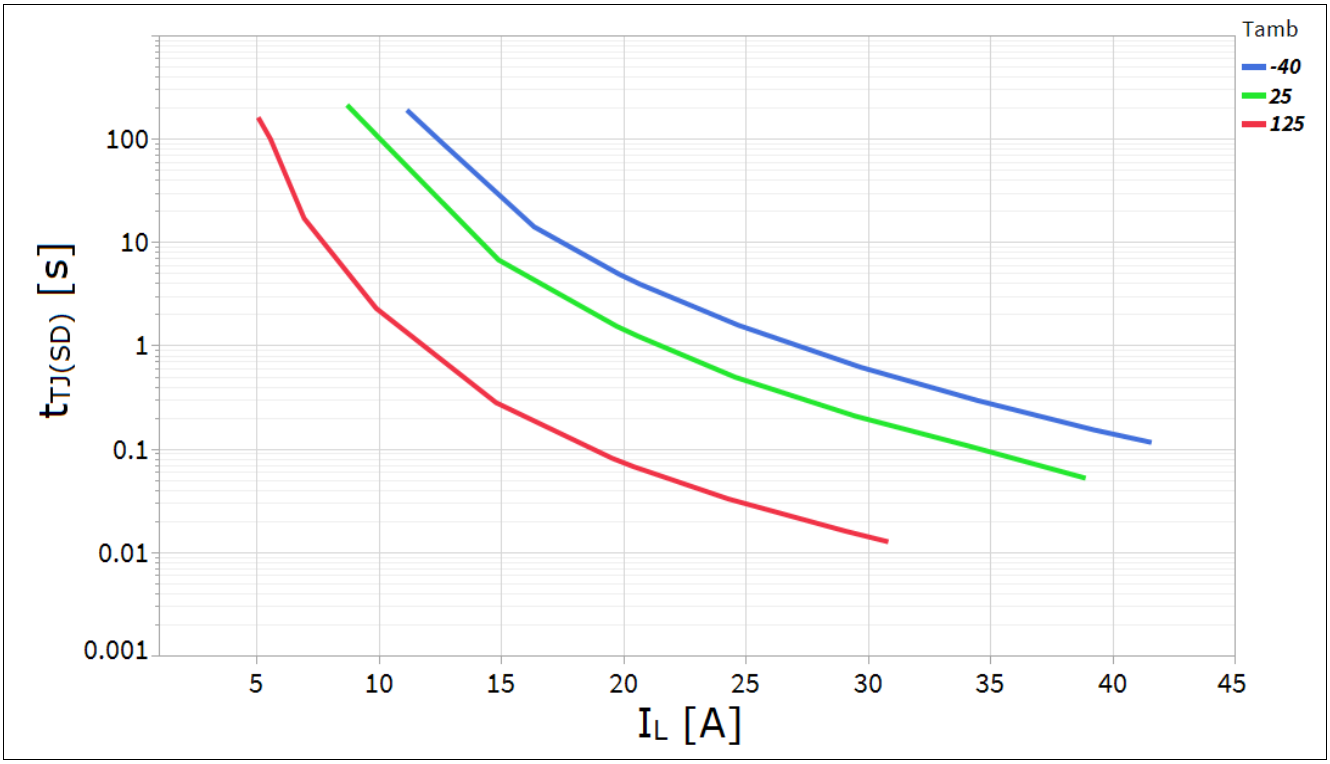


Figure 27 Typical *time to shut down* $t_{TJ(SD)}$ vs. I_L; V_{BAT}= 28V; V_{DD}= 5V; V_{IN}= 5V; $R_{thJA(1s0p+300mm^2)}$

9.3 Supply and Input Stage

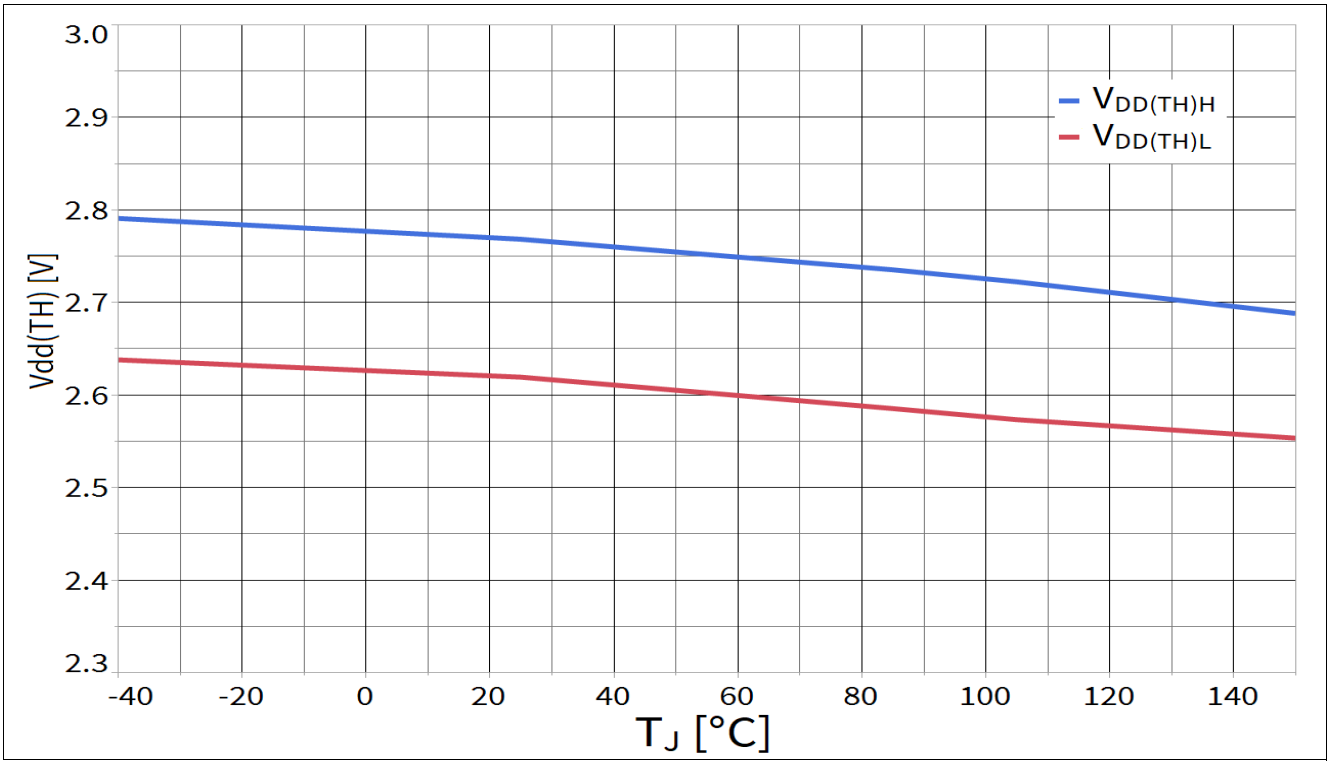


Figure 28 Typical $V_{DD(TH)}$ vs. T_J; $V_{DD(TH)H}$, $V_{DD(TH)L}$; V_{IN} = 3V;R_{SRP}= GND; V_{BAT} = 28V

Characterisation Results

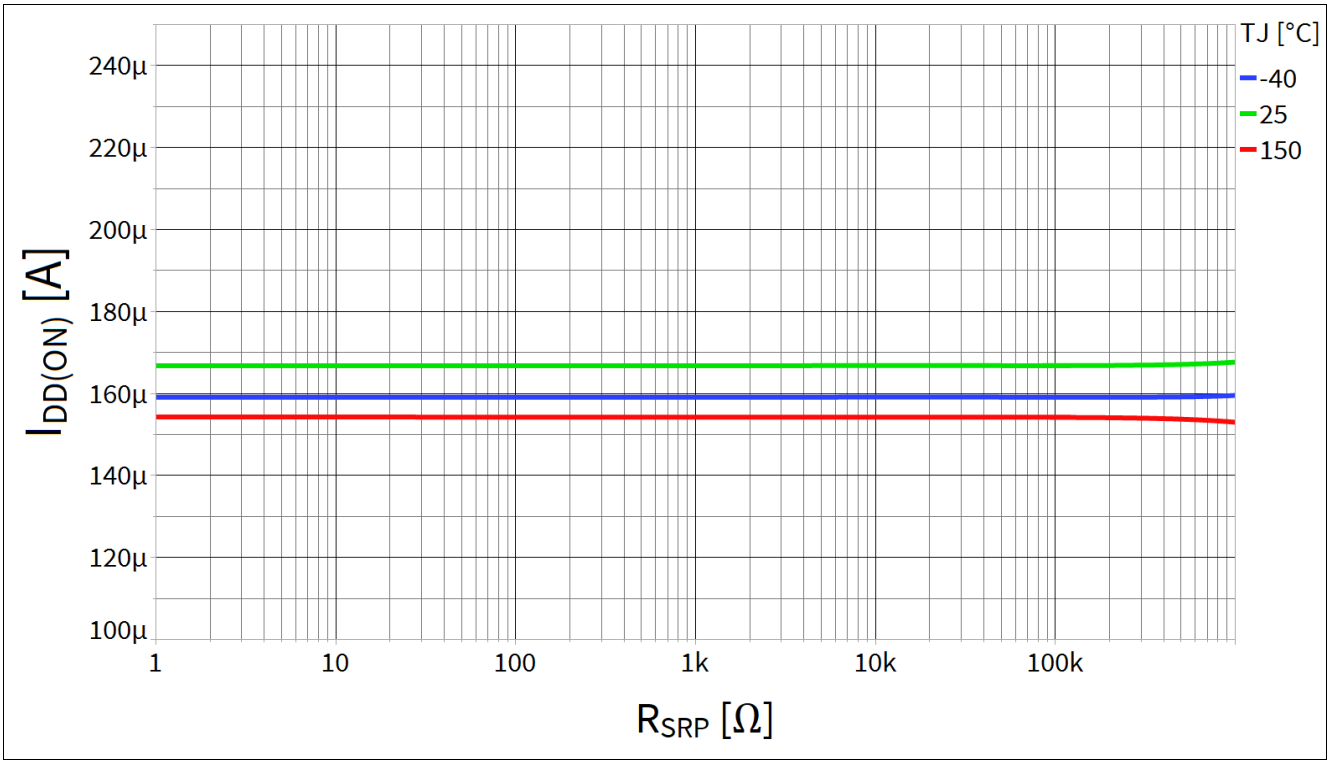


Figure 29 Typical $I_{DD(ON)}$ vs. R_{SRP}; I_L=$I_{L(NOM)}$; V_{IN} = 3V; V_{DD}= 5V; V_{BAT}=28V

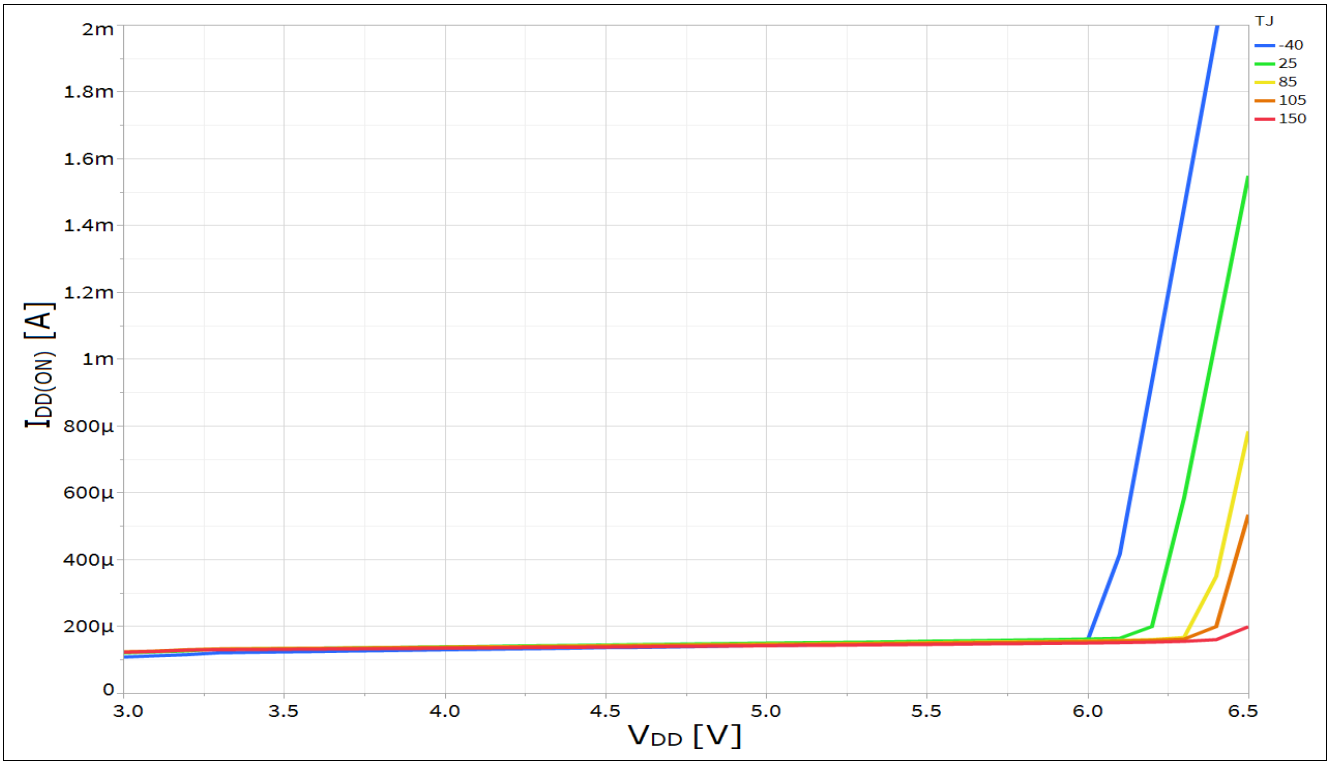


Figure 30 Typical $I_{DD(ON)}$ vs. V_{DD}; I_L=$I_{L(NOM)}$; V_{IN} = 3V; V_{BAT} = 28V; R_{SRP} = GND

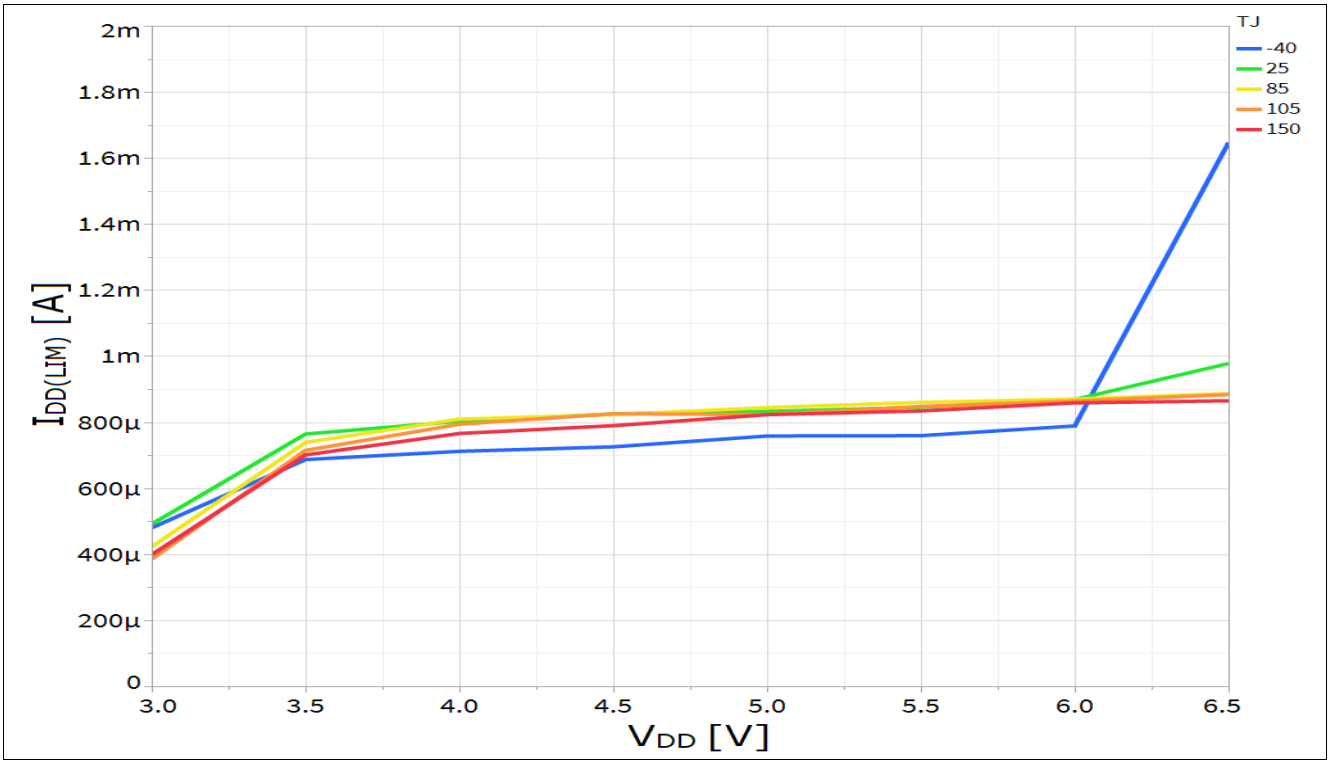


Figure 31 Typical $I_{DD(LIM)}$ vs. V_{DD}; V_{IN} = 3V; R_{SRP}= GND; V_{BAT}= 5V

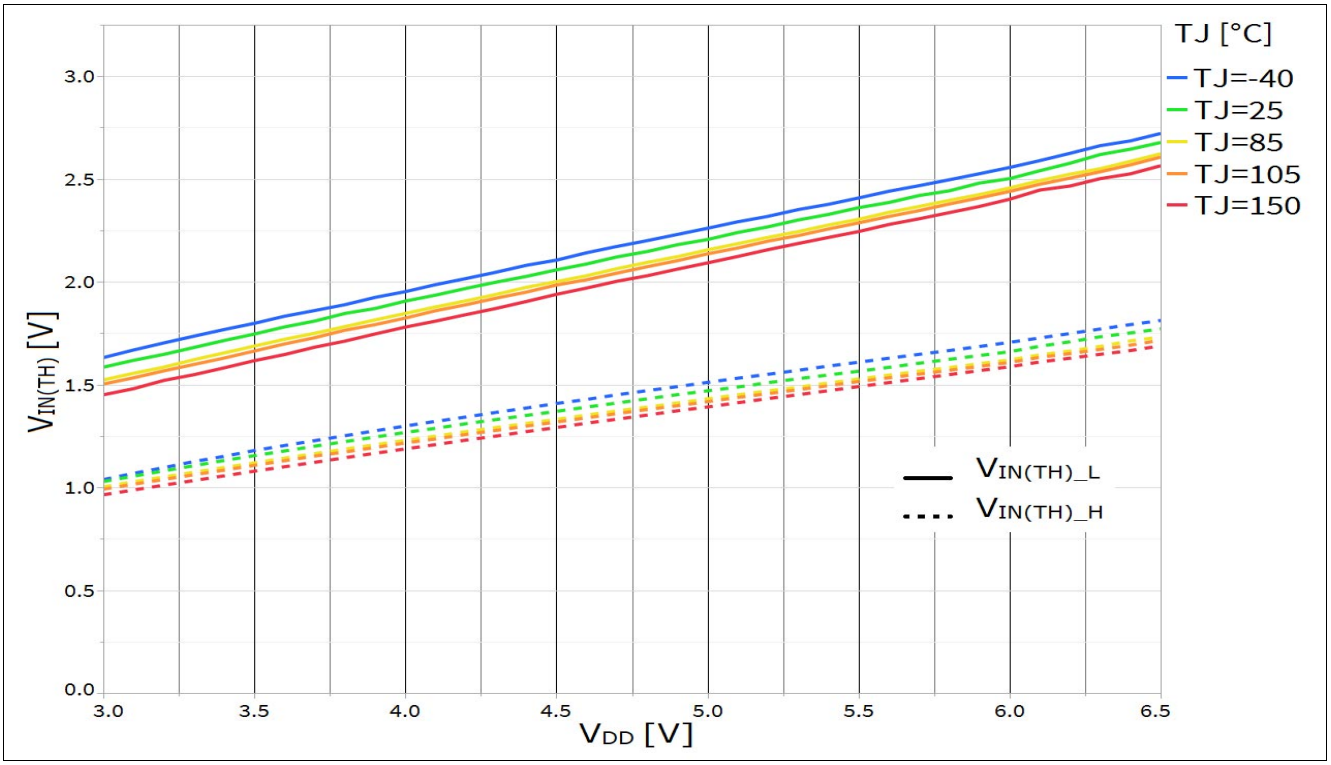


Figure 32 *Typical* $V_{IN(TH)}$ vs. V_{DD} ; $V_{IN(TH)H}$, $V_{IN(TH)L}$; R_{LOAD} = 150kΩ; R_{SRP} =GND; V_{BAT} = 28V

10 Application Information

10.1 Layout recommendations/considerations

As consequences of the fast switching times for high currents (I_{NOM} and above), special care has to be taken for the PCB layout. Stray inductances have to be minimized. BTT3018EJ has no separate pin for power ground and logic ground.

It is recommended:

- to ensure that the offset between the ground connection of the SRP resistor and ground pins of the device is minimized. R_{SRP} should be placed next to the device and directly connected to the GND pins, to avoid any influence of GND shift to SRP functionality.

- to ensure that the offset between the ground of the V_{DD} suplly and the ground of the pins of the device is minimized.

The maximum parasitic capacitance between the SRP line and GND (C_{SRP}) has to be less than 10pF to avoid any influence on SRP functionality (e.g. switching times).

10.2 Application Diagrams

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

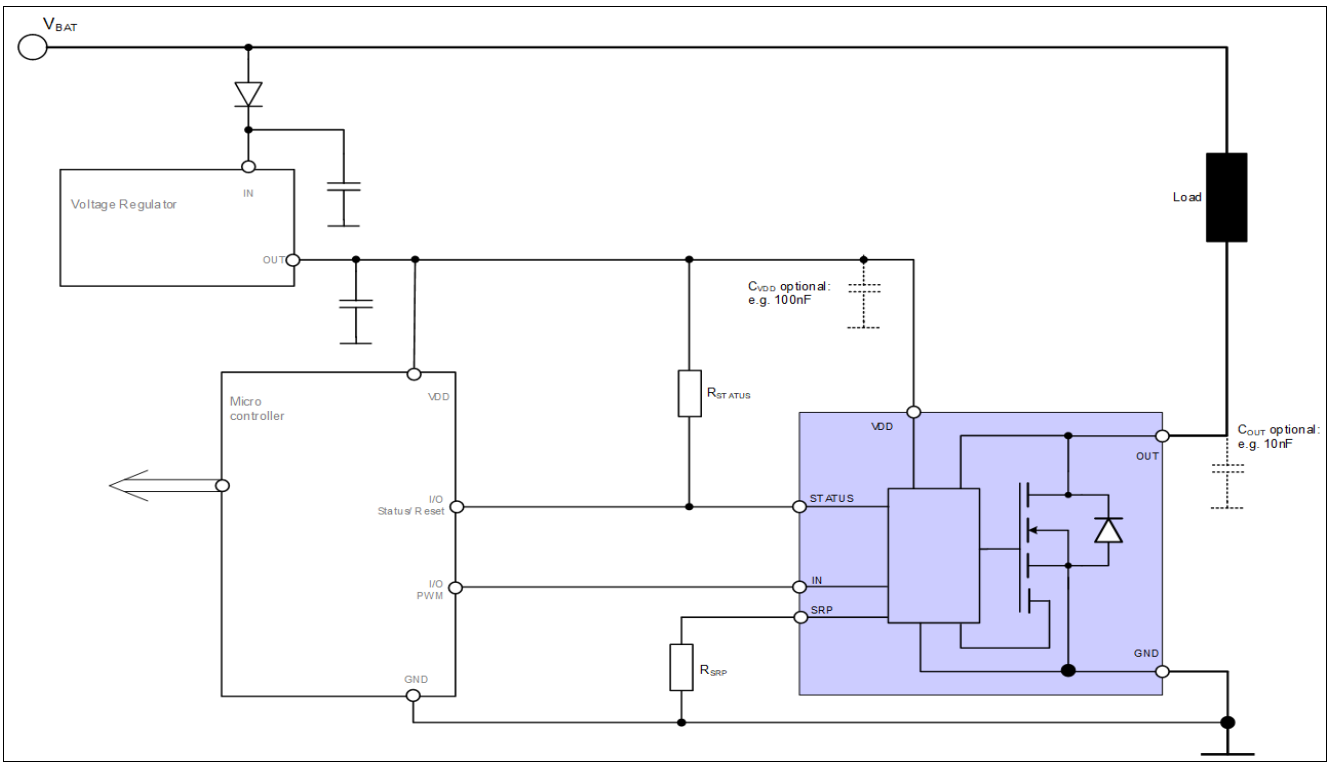


Figure 33 Application Diagram to use IN pin and STATUS pin independently

Recommended values for $V_{IN} = V_{DD} = 5$ V:

$R_{STATUS} = 100$ kΩ

Table 9 R_{SRP} switching modes[1)]

R_{SRP} min	R_{SRP} max	Unit	Behavior
0	2.2	kΩ	Fast switching mode. SRP pin can be connected to GND
2.2	160	kΩ	Adjustable switching mode
160	1000	kΩ	Slow switching mode

1) For switching timings please refer to **Chapter 8.1**

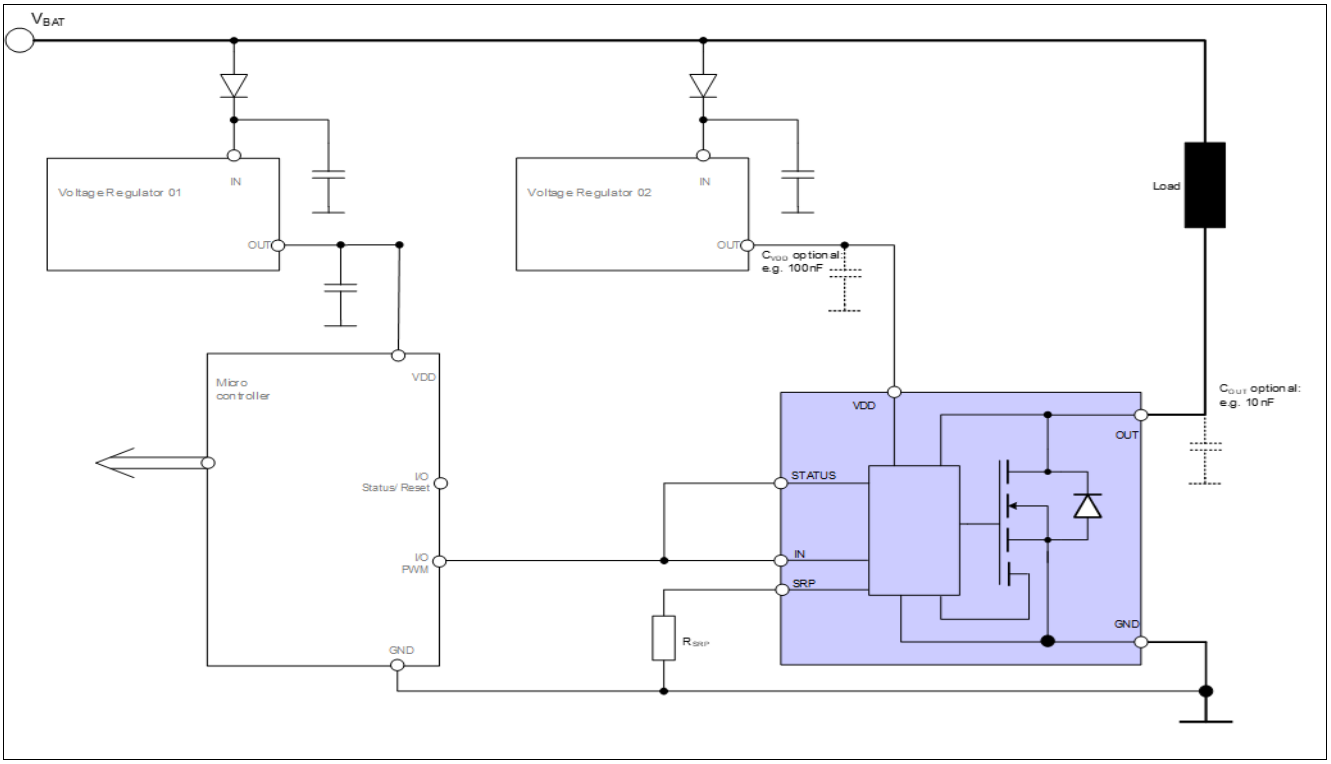


Figure 34 Application Diagram to use IN pin and STATUS pin simultaneously with different supply and microcontroller voltage class

Example given for V_{IN} = 3.3V; V_{DD} = 5V allows to mantain an optimal $R_{DS(ON)}$ while driving the input with a 3.3V microcontroller. This configuration makes not possible the readout of the fault signal and will reset the latch OFF via IN pin (see parameters in **Chapter 8.4**).

For R_{SRP} recommended values, please see **Table 9**

Note: This are very simplified examples of an application circuit. The function must be verified in the real application.

11 Package Outlines

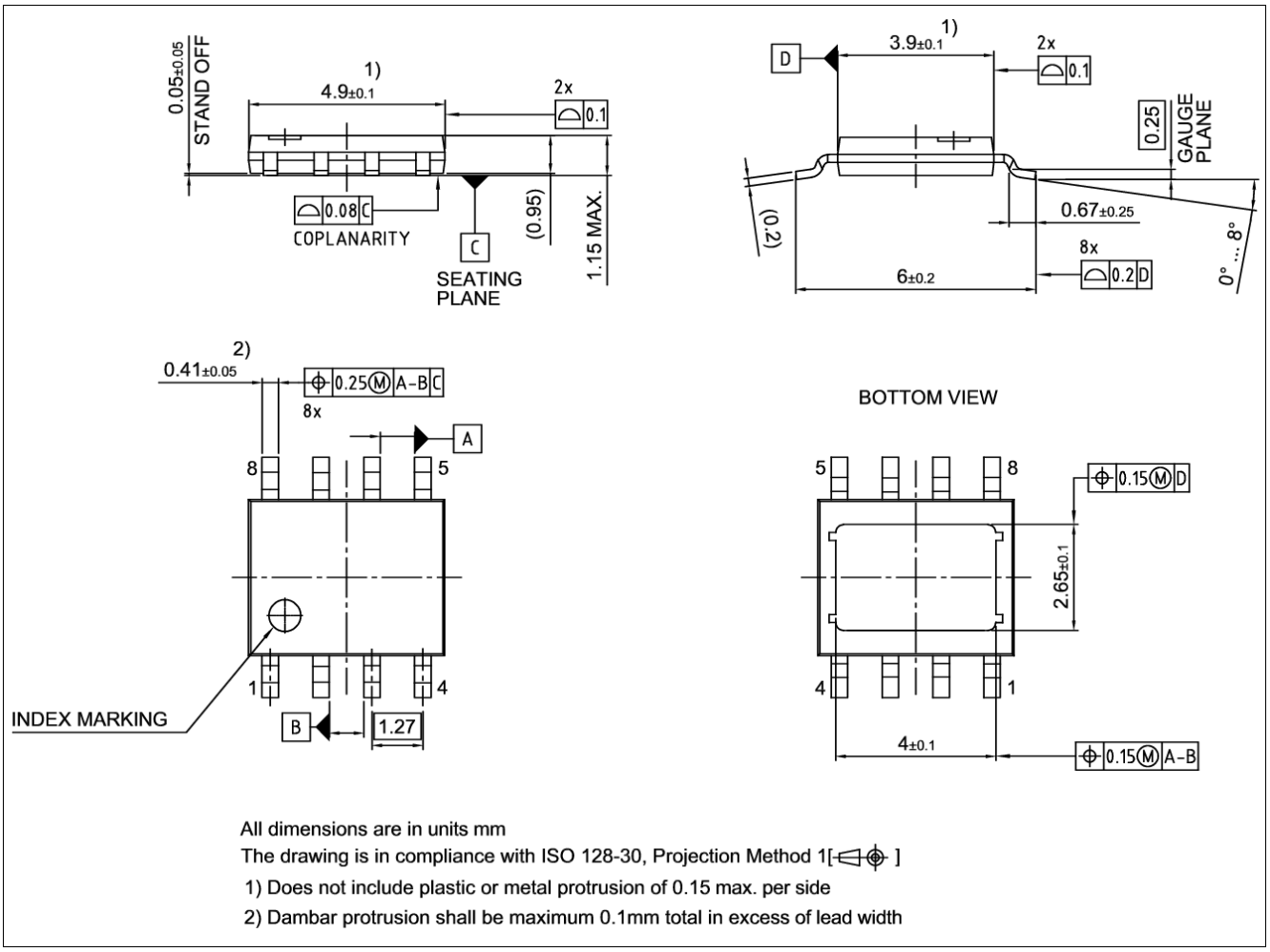


Figure 35 PG-TDSO-8

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

12 Revision History

Revision History

Revision	Date	Changes
Rev. 1.0	2020-01-17	Initial release

Edition 2020-01-16
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com