This anomaly list describes the known anomalies and workarounds for the AD7124-4/AD7124-8 released silicon. The anomalies listed apply to all AD7124-4 and AD7124-8 packaged material that is branded as follows:

AD7124-4BCPZ

AD7124-4BRUZ

AD7124-8BCPZ

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

AD7124-4 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Package Marking(s)	Silicon Status	Anomaly Sheet Revision	Date	No. of Reported Anomalies
Rev1p1	N/A		released	Rev0	7/1/2016	1

ANOMALIES

AD7124-4/AD7124-8 Functionality Issues

Table 1. Changing multiple mode bits in a single ADC_Control Register Write [er001]

Background	When two or more of the mode bits in the ADC_Control register are changed in a single write operation, the ADC may see a temporary value. If the temporary value is a calibration mode, a calibration is performed and cannot be aborted.
Anomaly	The serial interface is asynchronous to the internal master clock. The internal master clock rising edge is used to latch information from registers into the ADC controller. If the mode bits are updated at the same instant as an internal clock rising edge, the ADC_Control register reads the correct value. However, the data may not have settled when it is latched into the ADC controller on the internal clock rising edge. There may be a temporary corrupt value, consisting of the old values for some of the mode bits and the new value for other mode bits. On the next rising edge of the internal clock, the correct value is read by the ADC controller.
	If the temporary value is a single convert, idle mode, standby mode, the ADC controller will correct itself when it receives the settled mode value. However, if the temporary corrupt value is the mode setting for a calibration, the state machine within the AD7124 begins the calibration. It ignores the mode bit settings until the calibration is complete and it has set the ADC to idle mode.
Workaround	To prevent these unintended calibrations occurring, ADI recommend that only one of the mode bits be changed in any single write to the ADC_Control register. This ensures that the temporary state is either the old mode or the newly selected mode.
	Note: only the mode bits can be temporarily incorrect.
	Any bits related to conversions (gain, output data rate, filter type, for example) cause the sampling process to reset. So, these bits have settled to their final values when accessed.
	The power mode bits and the master clock select bits cause the ADC to reset, ensuring the bits have settled to their final value when accessed.
	Bits that control auxiliary functions such as general purpose outputs and excitation currents are never synchronised with the internal clock, they are transferred to the appropriate block using a signal derived from the serial clock SCLK.
	The bits that control the LDO capacitor check diagnostic are latched in a synchronised manner, ensuring settled bits are read.
	All other functionality on the AD7124-4/AD7124-8 is single bit controlled.
Related Issues	None

SECTION 1. PART NUMBER FUNCTIONALITY ANOMALIES

Reference Number	Description	Status
er001	Changing multiple mode bits in a single ADC_Control register write	Open

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