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# FDG332PZ

## P-Channel PowerTrench® MOSFET

-20V, -2.6A, 97mΩ

### Features

- Max  $r_{DS(on)}$  = 95mΩ at  $V_{GS} = -4.5V$ ,  $I_D = -2.6A$
- Max  $r_{DS(on)}$  = 115mΩ at  $V_{GS} = -2.5V$ ,  $I_D = -2.2A$
- Max  $r_{DS(on)}$  = 160mΩ at  $V_{GS} = -1.8V$ ,  $I_D = -1.9A$
- Max  $r_{DS(on)}$  = 330mΩ at  $V_{GS} = -1.5V$ ,  $I_D = -1.0A$
- Very low level gate drive requirements allowing operation in 1.5V circuits
- Very small package outline SC70-6
- RoHS Compliant

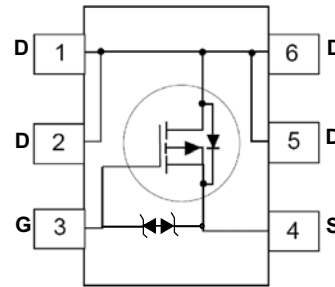
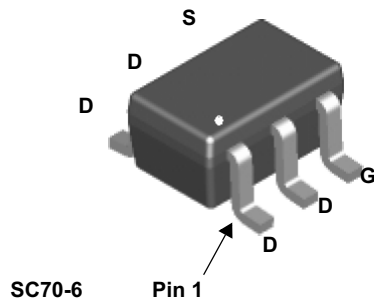


### General Description

This P-Channel MOSFET uses Fairchild's advanced low voltage PowerTrench® process. It has been optimized for battery power management applications.

### Applications

- Battery management
- Load switch



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	$\pm 8$	V
$I_D$	Drain Current -Continuous	-2.6	A
	-Pulsed	-9	
$P_D$	Power Dissipation (Note 1a)	0.75	W
	Power Dissipation (Note 1b)	0.48	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single operation (Note 1a)	170	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single operation (Note 1b)	260	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.2P	FDG332PZ	SC70-6	7"	8 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-13		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-0.4	-0.7	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		2.5		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{V}, I_D = -2.6\text{A}$		73	95	m $\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -2.2\text{A}$		90	115	
		$V_{GS} = -1.8\text{V}, I_D = -1.9\text{A}$		117	160	
		$V_{GS} = -1.5\text{V}, I_D = -1.0\text{A}$		147	330	
		$V_{GS} = -4.5\text{V}, I_D = -2.6\text{A}, T_J = 125^\circ\text{C}$		100	133	
$g_{FS}$	Forward Transconductance	$V_{DD} = -5\text{V}, I_D = -2.6\text{A}$		9		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		420	560	pF
$C_{oss}$	Output Capacitance			85	115	pF
$C_{rss}$	Reverse Transfer Capacitance			75	115	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{V}, I_D = -2.6\text{A}, V_{GS} = -4.5\text{V}, R_{GEN} = 6\Omega$		5.2	10	ns
$t_r$	Rise Time			4.8	10	ns
$t_{d(off)}$	Turn-Off Delay Time			59	95	ns
$t_f$	Fall Time			28	45	ns
$Q_g$	Total Gate Charge			7.6	10.8	nC
$Q_{gs}$	Gate to Source Charge	$V_{GS} = -4.5\text{V}, V_{DD} = -10\text{V}, I_D = -2.6\text{A}$		0.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.9		nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			-0.6	A	
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -0.6\text{A}$ (Note 2)		-0.7	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 2.6\text{A}, di/dt = 100\text{A}/\mu\text{s}$		28	45	ns
$Q_{rr}$	Reverse Recovery Charge			8	13	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



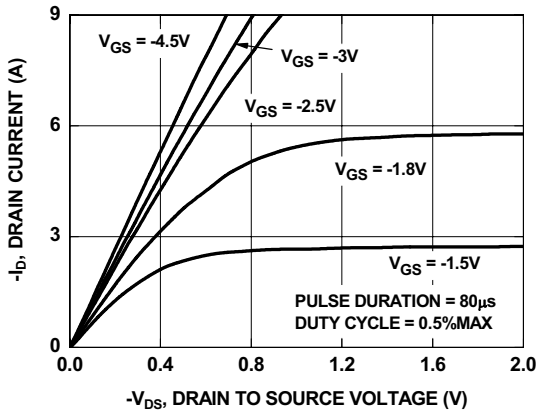
a.  $170^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.



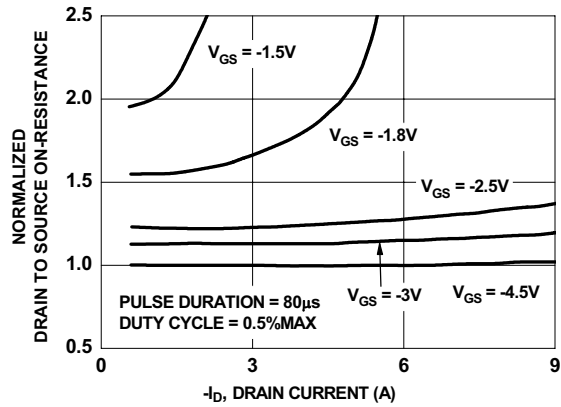
b.  $260^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty cycle < 2.0%.

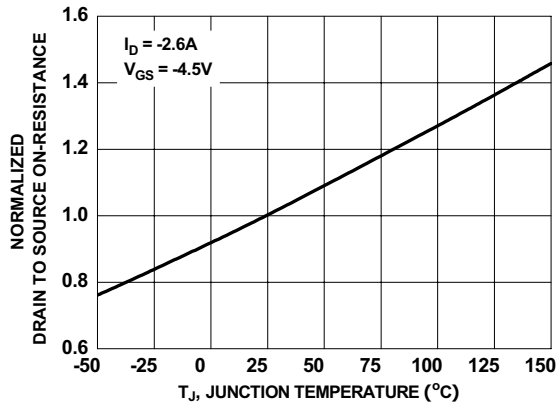
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



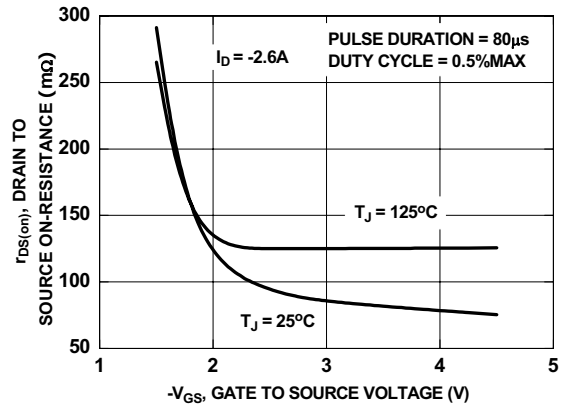
**Figure 1. On-Region Characteristics**



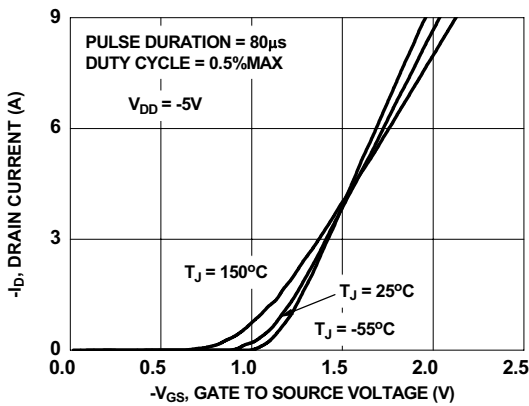
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



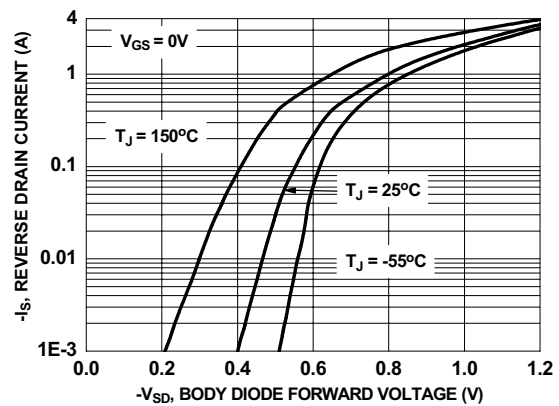
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

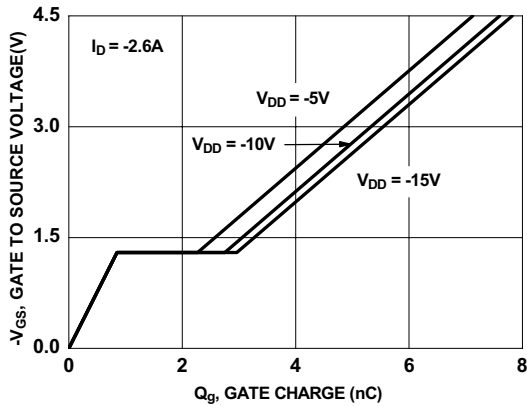


**Figure 5. Transfer Characteristics**

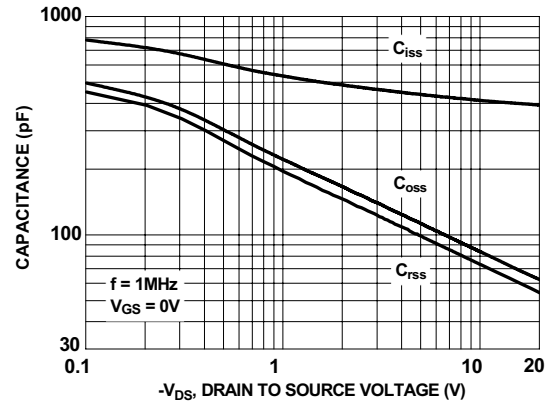


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

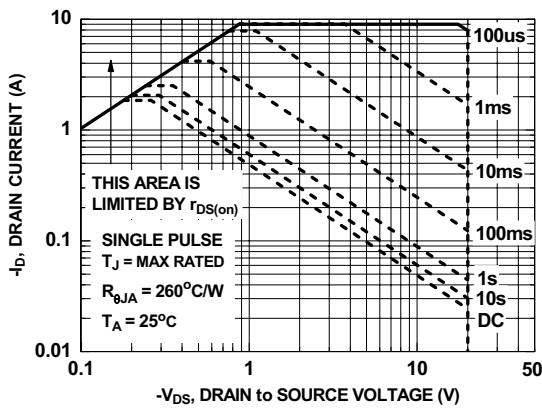
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



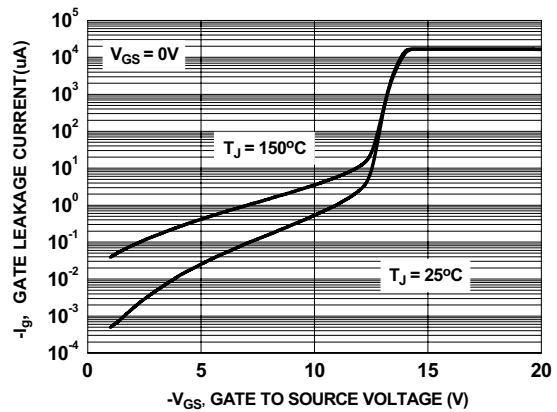
**Figure 7. Gate Charge Characteristics**



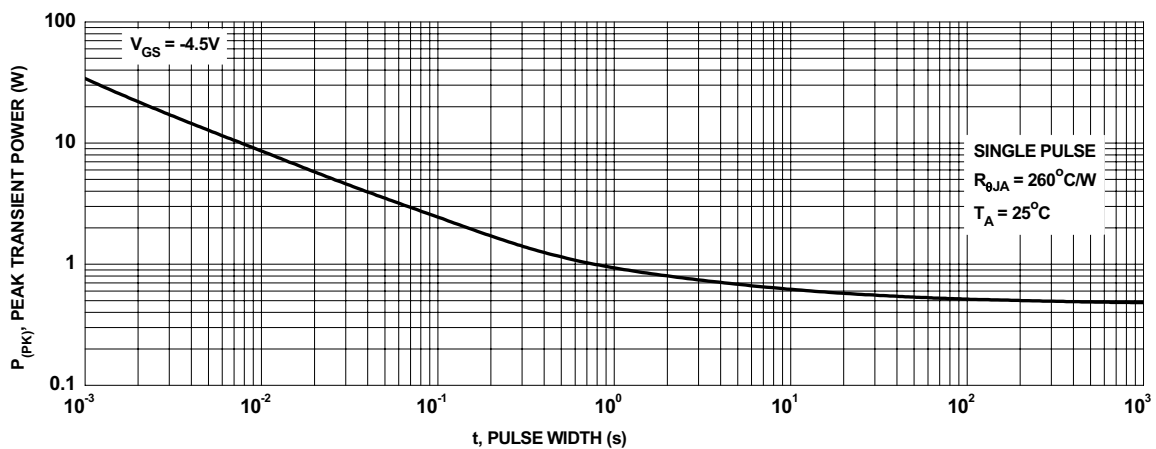
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

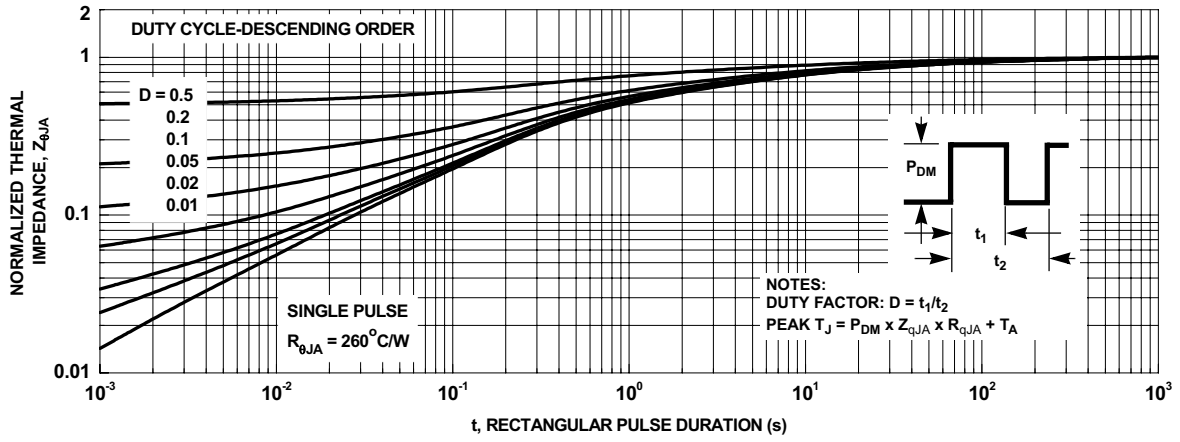


**Figure 10. Gate Leakage Current vs Gate to Source Voltage**



**Figure 11. Transient Thermal Response Curve**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted






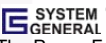


**Figure 12. Transient Thermal Response Curve**



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