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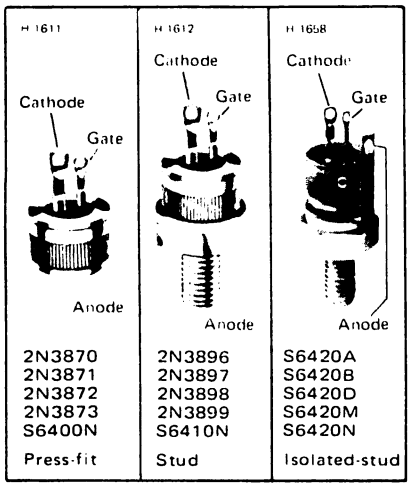
Thyristors
2N3870-2N3873,S6400N
2N3896-2N3899,S6410N
S6420A,B,D,M,N



2N3870	2N3896	S6420A
2N3871	2N3897	S6420B
2N3872	2N3898	S6420D
2N3873	2N3899	S6420M
S6400N	S6410N	S6420N
Press-fit	Stud	Isolated-stud

35-A Silicon Controlled Rectifiers

Press-Fit, Stud, and Isolated-Stud Packages

For Low-Voltage Operation—2N3870, 2N3896, S6420A
For 120-V Line Operation—2N3871, 2N3897, S6420B
For 240-V Line Operation—2N3872, 2N3898, S6420D
For High-Voltage Operation—2N3873, 2N3899, S6420M
S6400N S6401N S6420N

Features:

- High di/dt and dv/dt capabilities
- Low on-state voltage at high current levels
- Low thermal resistance
- Shorted-emitter gate-cathode construction . . . contains an internally diffused resistor between gate and cathode
- Center gate construction . . . provides rapid uniform gate-current spreading for faster turn-on with substantially reduced heating effects

These types are all-diffused, silicon controlled rectifiers (reverse-blocking triode thyristors) designed for power switching, power control, and voltage regulator applications and for heating, lighting, and motor speed-control circuits.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		2N3870 2N3896 S6420A	2N3871 2N3897 S6420B	2N3872 2N3898 S6420D	2N3873 2N3899 S6420M	S6400N S6410N S6420N	
*NON-REPETITIVE PEAK REVERSE VOLTAGE▲							
Gate Open	V_{RSOM}	150	330	660	700	900	V
NON-REPETITIVE PEAK OFF-STATE VOLTAGE▲							
Gate Open	V_{DSOM}	150	330	660	700	900	V
*REPETITIVE PEAK REVERSE VOLTAGE▲							
Gate Open	V_{RROM}	100	200	400	600	800	V
*REPETITIVE PEAK OFF-STATE VOLTAGE▲							
Gate Open	V_{DROM}	100	200	400	600	800	V
ON-STATE CURRENT:							
T_C = 65°C◆, conduction angle = 180°:							
RMS	$I_{T(RMS)}$	35					A
* Average	$I_{T(AV)}$	22					A
For other conditions		See Figs. 3 & 5					
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}						
For one full cycle of applied principal voltage							
* 60 Hz (sinusoidal)		350					A
50 Hz (sinusoidal)		300					A
For more than one full cycle of applied principal voltage		See Fig. 5					
RATE OF CHANGE OF ON-STATE CURRENT							
$V_D = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.5 μs (See Fig. 13)	di/dt	200					A/μs
FUSING CURRENT (for SCR protection):							
T_J = −40 to 100°C, t = 1 to 8.3 ms	I^2t	300					A^2s
GATE POWER DISSIPATION●:							
Peak Forward (for 10 μs max., See Fig. 8)	P_{GM}	40					W
Peak Reverse	P_{RGM}	See Fig. 9					
Average (averaging time = 10 ms max.)	$P_{G(AV)}$	0.5					W
*TEMPERATURE RANGE■:							
Storage		−40 to 125					°C
Operating (Case)		−40 to 100					°C
TERMINAL TEMPERATURE (During soldering):	T_T						
For 10 s max. (terminals and case)		225					°C

* In accordance with JEDEC registration data filed for the JEDEC (2N-series) types.
▲ These values do not apply if there is a positive gate signal. Gate must be open or negatively biased.
◆ T_C = 60° for isolated-stud package types.
● Any product of gate current and gate voltage which results in a gate power less than the maximum is permitted.
■ Temperature measurement point is shown on the DIMENSIONAL OUTLINE.

ELECTRICAL CHARACTERISTICS

At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

CHARACTERISTIC	SYMBOL	LIMITS FOR ALL TYPES Unless Otherwise Specified			UNITS
		MIN.	TYP.	MAX.	
Peak Off-State Current: (Gate open, T_C = 100°C) Forward Current (I_{DOM}) at $V_D = V_{DROM}$ Reverse Current (I_{ROM}) at $V_R = V_{RROM}$	I_{DOM} or I_{ROM}				
2N3870, 2N3896, S6420A		–	0.2	2*	mA
2N3871, 2N3897, S6420B		–	0.25	2.5*	mA
2N3872, 2N3898, S6420D		–	0.3	3*	mA
2N3873, 2N3899, S6420M, S6400N, S6410N, S6420N		–	0.35	4*	mA
Instantaneous On-State Voltage:	v_T				
i_T = 69 A (peak), T_C = 25°C		–	–	1.85*	V
i_T = 100 A (peak), T_C = 25°C		–	1.7	2.1	V
DC Gate Trigger Voltage:	V_{GT}				
V_D = 12 V (dc), R_L = 30 Ω, T_C = -40°C		–	1.5	3*	V
V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C		–	1.1	2	V
For other case temperatures		See Fig. 11			
DC Gate Trigger Current:	I_{GT}				
V_D = 12 V (dc), R_L = 30 Ω, T_C = -40°C		–	46	80*	mA
V_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C		1	25	40	mA
For other case temperatures		See Fig. 10			
Instantaneous Holding Current: Gate open, T_C = 25°C	i_{HO}	0.5	30	70	mA
For other case temperatures		See Fig. 7			
Gate Controlled Turn-On Time: (Delay Time + Rise Time) For $V_D = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.1 μs, I_T = 30 A (peak), T_C = 25°C (See Fig. 12 & 14.)	t_{gt}	–	1.25	2	μs
Circuit Commutated Turn-Off Time: $V_D = V_{DROM}$, i_T = 18 A, pulse duration = 50 μs, dv/dt = 20 V/μs, -di/dt = -30 A/μs, I_{GT} = 200 mA, T_C = 80°C (See Fig. 15.)	t_q	–	20	40	μs
Critical Rate of Rise of Off-State Voltage: $V_D = V_{DROM}$, exponential voltage rise, Gate open, T_C = 100°C (See Fig. 16.)	dv/dt	10	100	–	V/μs
Thermal Resistance, Junction-to-Case: Steady-State	$R_{\theta JC}$				
Press-fit & stud types		–	–	0.9*	°C/W
Isolated-stud types		–	–	1	°C/W

*In accordance with JEDEC registration data filed for the JEDEC (2N-series) types.

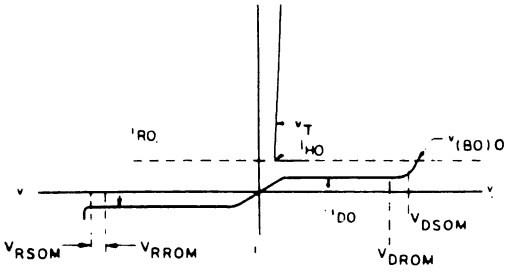


Fig.1—Principal voltage-current characteristic.

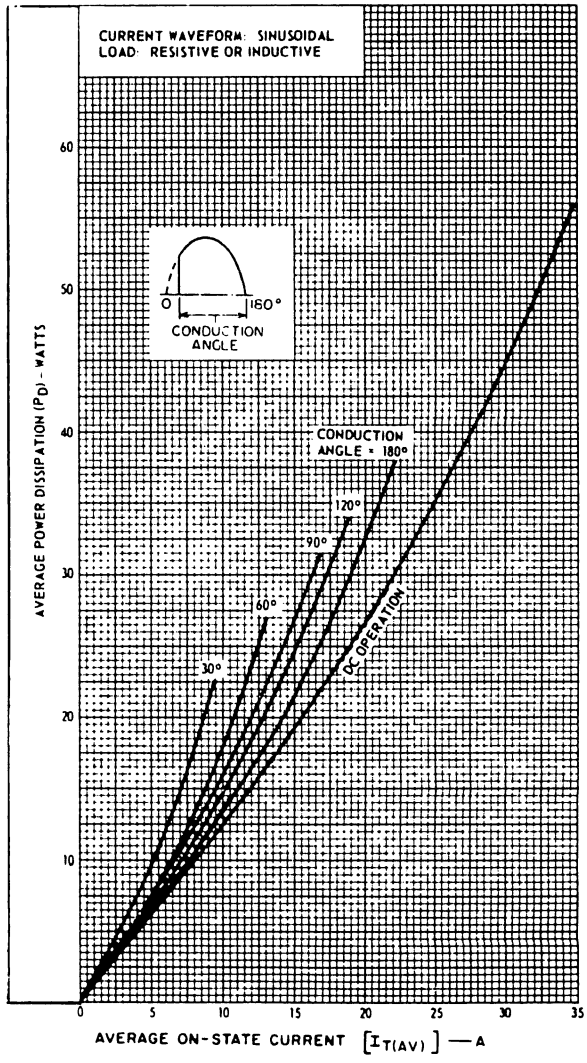


Fig.2—Power dissipation vs. on-state current.

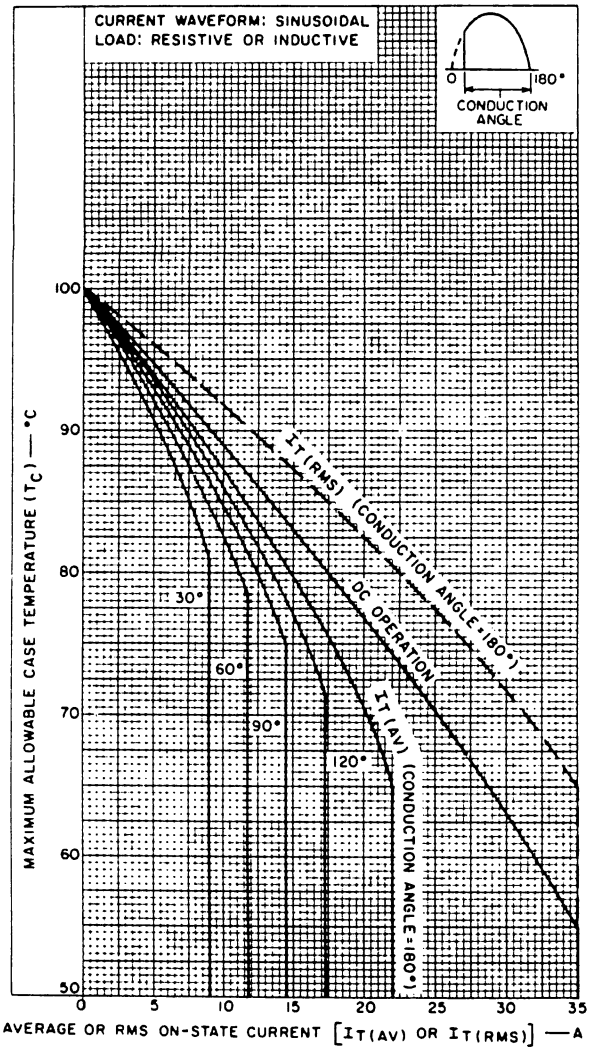


Fig.3—Maximum allowable case temperature vs. on-state current for press-fit and stud types.

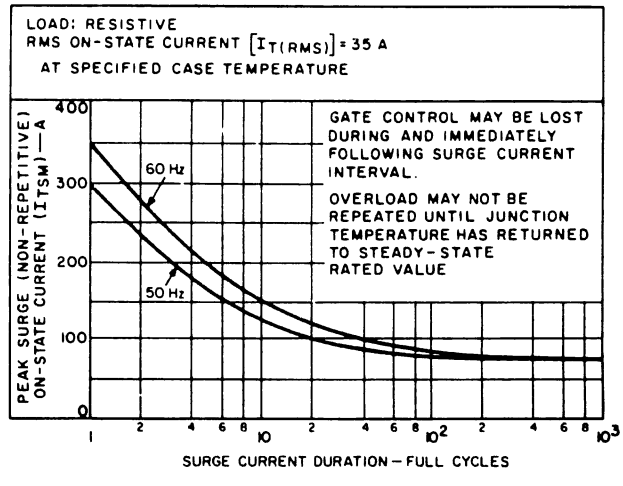


Fig.4 —Peak surge on-state current vs. surge current duration.

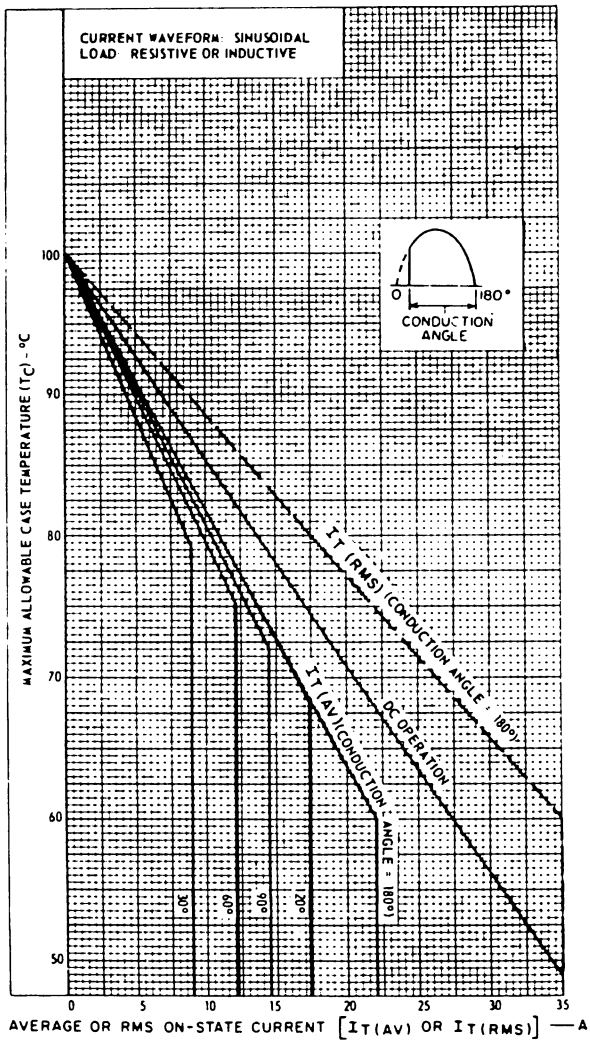


Fig.5—Maximum allowable case temperature vs. on-state current for isolated-stud types.

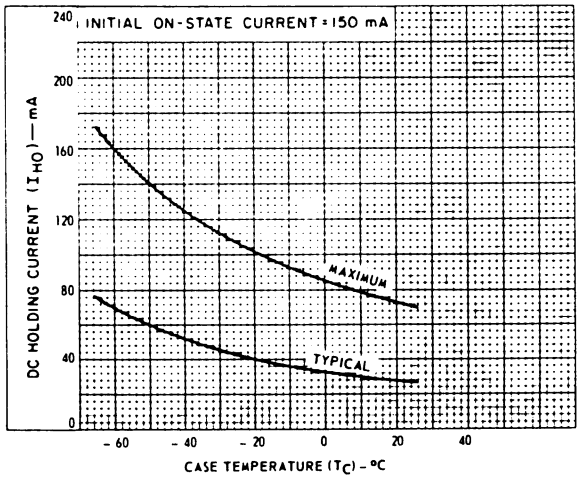


Fig.7—DC holding current vs. case temperature.

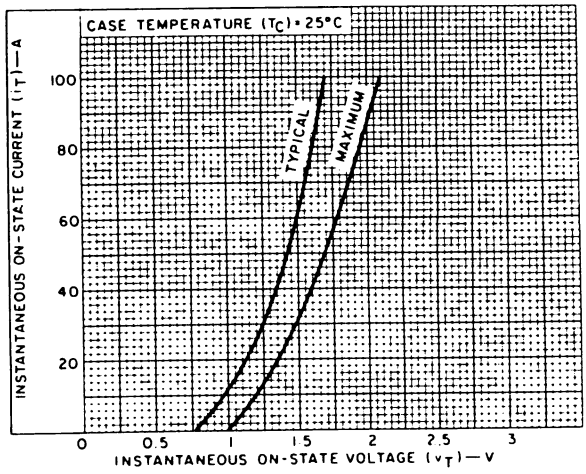


Fig.6—Instantaneous on-state current vs. on-state voltage.

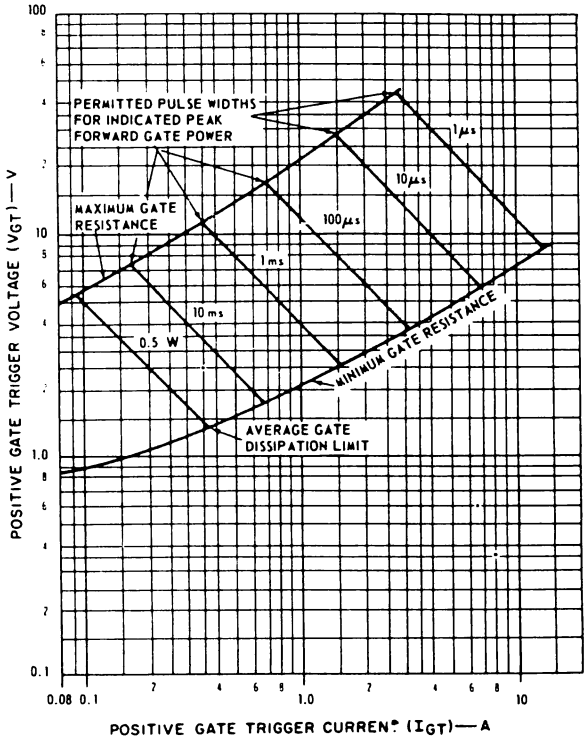


Fig.8—Gate pulse characteristics for forward triggering mode.

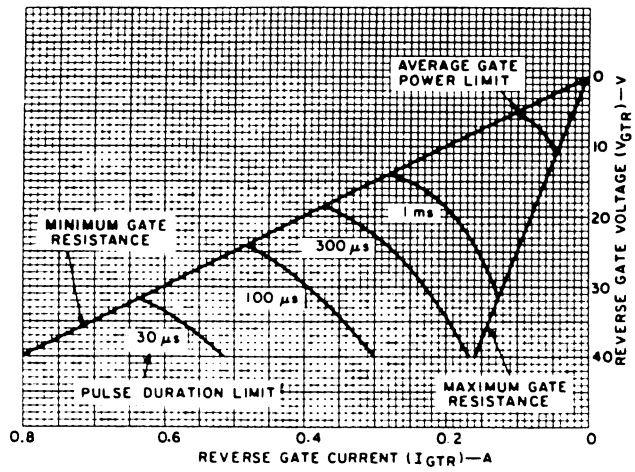


Fig.9—Reverse gate voltage vs. reverse gate current.

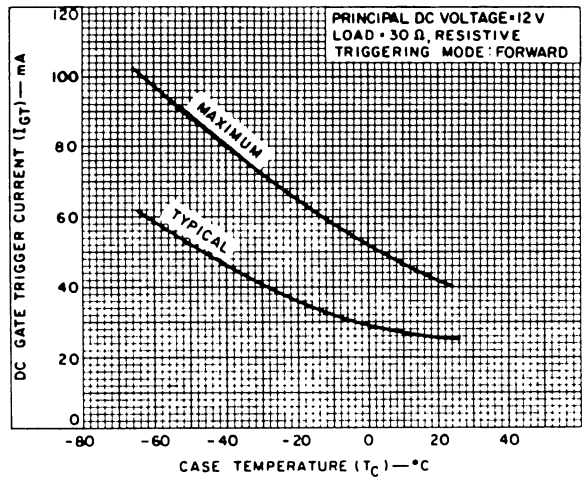


Fig.10—DC gate trigger current (forward) vs. case temperature.

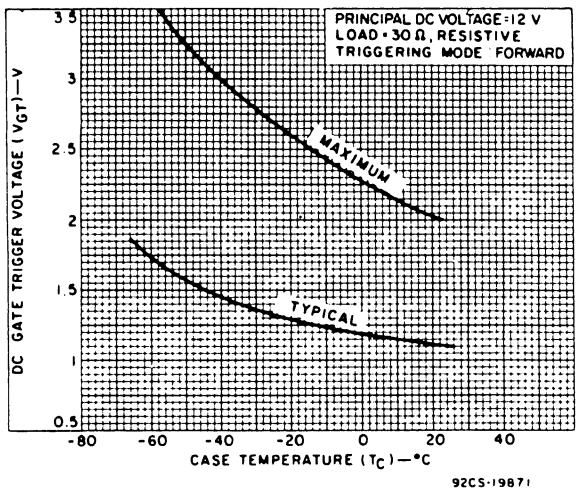


Fig.11—DC gate trigger voltage (forward) vs. case temperature.

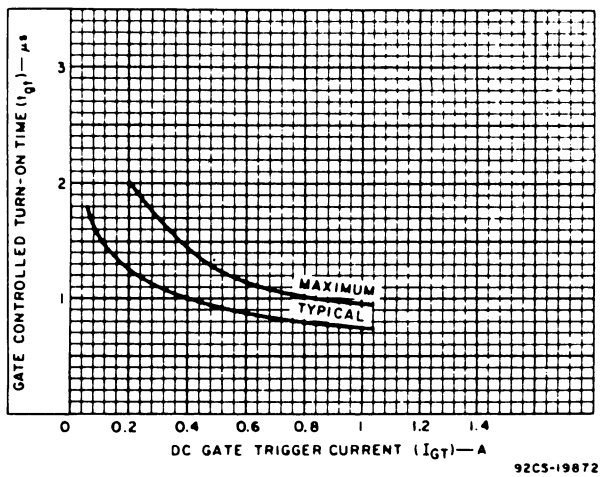


Fig.12—Gate-controlled turn-on time vs. gate trigger current.

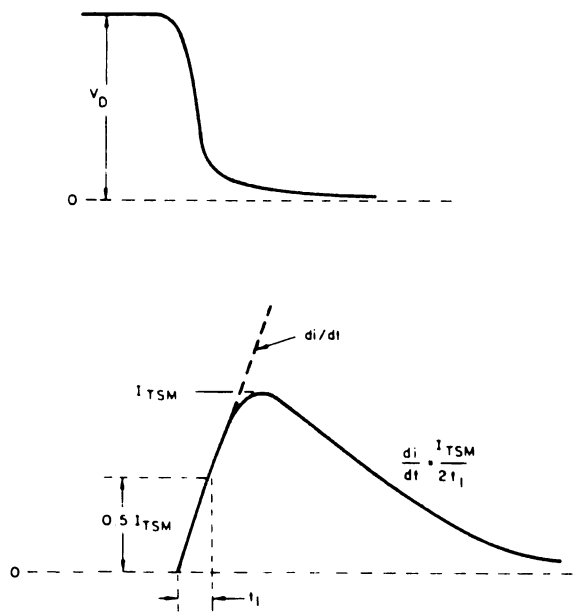


Fig.13—Rate of change of on-state current with time (defining di/dt).

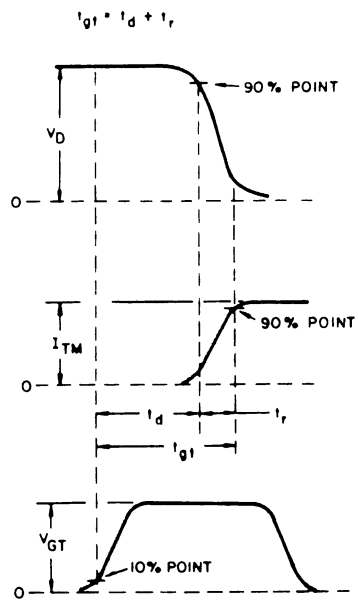


Fig.14—Relationship between off-state voltage, on-state current, and gate trigger voltage showing reference points for definition of turn-on time (t_{gt}).

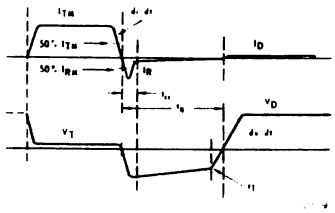


Fig.15—Relationship between instantaneous on-state current and voltage showing reference points for definition of circuit commutated turn-off time (t_q).

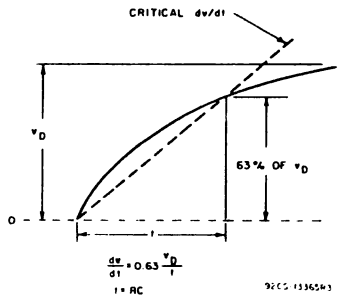
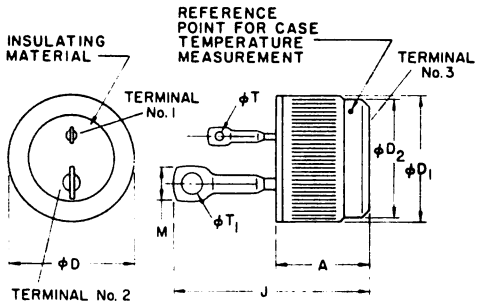


Fig.16- Rate of rise of off-stage voltage with time (defining critical dv/dt).

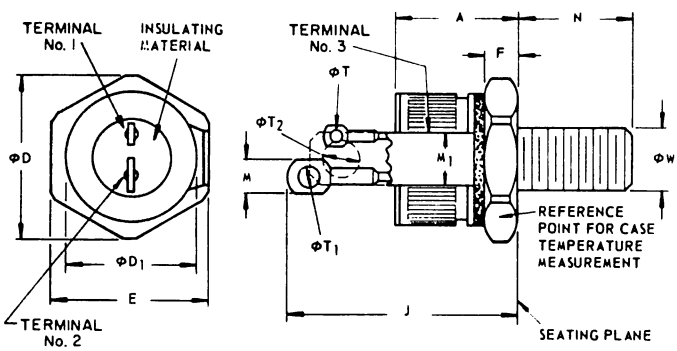
DIMENSIONAL OUTLINE FOR TYPES 2N3870, 2N3871, 2N3872, 2N3873, S6400N PRESS-FIT



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.380	–	9.65	
φD	0.501	0.510	12.73	12.95	
ϕD_1	–	0.505	–	12.83	2
ϕD_2	0.465	0.475	11.81	12.07	
J	–	0.750	–	19.05	
M	–	0.155	–	3.94	1
φT	0.058	0.068	1.47	1.73	
ϕT_1	0.080	0.090	2.03	2.29	

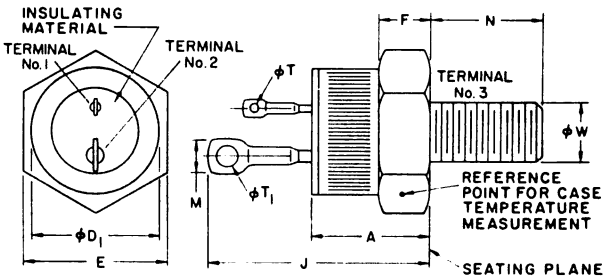
NOTES:
1. Countour and angular orientation of these terminals is optional.
2. Outer diameter of knurled surface.

DIMENSIONAL OUTLINE FOR TYPES S6420A, B, D, M, N ISOLATED-STUD



NOTES:
1. Contour and angular orientation of these terminals is optional.
2. φW is pitch diameter of coated threads, Ref: ASA B_1, 1-1960. Recommended torque: 50 inch-pounds.
3. A chamfer or undercut on one or both ends of hexagonal portion is optional.

DIMENSIONAL OUTLINE FOR TYPES 2N3896, 2N3897, 2N3898, 2N3899, S6410N STUD



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.330	0.505	8.4	12.8	
ϕD_1	–	0.544	–	13.81	
E	0.544	0.562	13.82	14.28	
F	0.113	0.200	2.87	5.08	3
J	–	0.950	–	24.13	
M	–	0.155	–	3.94	1
N	0.422	0.453	10.72	11.50	
φT	0.058	0.068	1.47	1.73	
ϕT_1	0.080	0.090	2.03	2.29	
φW	1/4-28 UNF-2A		1/4-28 UNF-2A		2

NOTES:
1. Contour and angular orientation of these terminals is optional.
2. φW is pitch diameter of coated threads, Ref: ASA B_1, 1-1960. Recommended torque: 50 inch-pounds.
3. A chamfer or undercut on one or both ends of hexagonal portion is optional.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.673	–	17.09	
φD	0.604	0.614	15.34	15.59	
ϕD_1	0.501	0.505	12.72	12.82	
E	0.551	0.557	13.99	14.14	
F	0.175	0.185	4.44	4.69	3
J	–	1.055	–	26.79	
M	–	0.155	–	3.94	1
M_1	0.200	0.210	5.08	5.33	1
N	0.422	0.452	10.72	11.48	
φT	0.058	0.068	1.47	1.73	
ϕT_1	0.080	0.090	2.03	2.29	
ϕT_2	0.138	0.148	3.50	3.75	
φW	1/4-28 UNF-2A		1/4-28 UNF-2A		2

TERMINAL CONNECTIONS FOR ALL TYPES

No. 1 – Gate
No. 2 – Cathode
Case, No. 3 – Anode